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Cromemco

68000 Board Family

Instruction Manual

Cromemco®

68000 Board Family

Instruction Manual

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SCHEMATICS

DPU
MCU
256MSU
512MSU

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Chapter 1

INTRODUCTION

The Cromemco 68000 board family is comprised of the **DPU** Dual Processor Unit, **MCU** Memory Control Unit, and **256MSU** & **512MSU** Memory Storage Units.

Based on the Motorola **MC68000** microprocessor chip, the Cromemco **DPU** introduces **32-bit** computing speed and power to the Cromemco line of computers. The DPU is a Dual Processor Unit, also incorporating an 8-bit **Z-80A** microprocessor chip to ensure compatibility with existing software. Microprocessor selection is under software control, allowing the programmer to select the chip of choice for any particular application or routine. An existing Z-80 program, for example, may be run on the DPU with a subroutine or two rewritten in 68000 code to speed things up.

And what about that program which doesn't quite all fit in main memory? With a 24-bit wide address bus, the MC68000 can address up to 16 Mbytes of memory. This is not bank-selected memory. The MC68000 can **directly address each byte in up to 16 megabytes** of RAM.

The Cromemco **MCU** Memory Controller Unit acts as an interface between the S-100/IEEE-696 bus and the Cromemco **M bus** which connects the MCU to its associated MSUs. A single MCU works in conjunction with up to two MSU boards providing not only an interface, but an error detection, correction, and logging system.

The Cromemco **256MSU** provides 128K 22-bit words, each of which includes six bits for error detection and correction. The **512MSU** provides 256K 22-bit words. This scheme allows all single-bit errors to be corrected and logged, and double-bit errors to be detected and logged.

The Cromemco 68000 board family **conforms to the S-100/IEEE-696** bus standard.

Chapter 2

THE DPU DUAL PROCESSOR UNIT

INTRODUCTION

The Cromemco DPU Dual Processor Unit incorporates two microprocessors on a single board. The MC68000 provides the power and speed of a new generation of 32 bit microprocessor chips while the Z-80A guarantees compatibility with most existing hardware and software. One of the two microprocessors is in charge of the bus at any given point in time, yielding control to the other as required by the software.

The MC68000 microprocessor has 32-bit wide internal registers, a 16-bit wide external data bus, and a 24-bit wide external address bus. It can directly address 16 megabytes of memory and has 56 instruction types, 5 data types, and 14 address modes yielding an instruction set comprised of over 1000 instructions. These features make the MC68000 extremely fast and versatile.

The Z-80A allows the DPU to maintain compatibility with most existing Cromemco hardware and software. The DPU can be used as a direct replacement for a ZPU board.

Table 2-1 shows the operational specifications for the DPU board.

Table 2-1: DPU SPECIFICATIONS

Processors:	MC68000 and Z-80A
Clock Rate:	MC68000 - 8MHz Z-80A - 4MHz System - 4MHz
Instruction Set:	MC68000 - over 1000 instructions in 56 main types Z-80A - 158 instructions including the 78 instructions of the 8080 processor
Power-on Jump:	Jumper selectable to any 4K memory boundary within the first 64K page. Preselected for standard Cromemco systems.
Processor Control:	Software controlled switching between MC68000 and Z-80A.
Bus:	S-100/IEEE-696
Power Requirements:	+8 volts @ 2.0 amps
Operating Environment:	0 to 55 degrees C

SETUP AND INSTALLATION

Switch Settings

There are no switches on the DPU.

Jumper Selectable Options

The Cromemco DPU board is ready to be used in your Cromemco system as it is shipped from the factory. There are three jumpers which may be used for experimental purposes. The locations of these jumpers are shown in Figure 2-1.

Bus Selection Jumper - This jumper is not needed when using Cromemco boards.

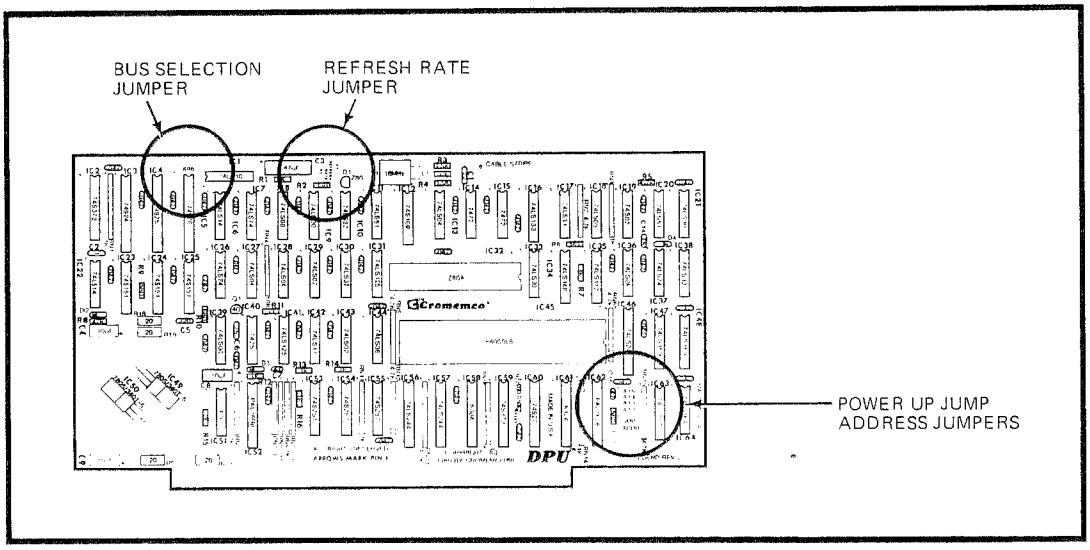

Figure 2-1: DPU JUMPER LOCATIONS

Memory Refresh Rate - This jumper is not needed when using Cromemco boards. As shipped from the factory, there is a trace between the common node and the X2 solder pad. During MC68000 operation, this causes a refresh cycle to be inserted approximately every 16 microseconds. Cutting this trace and installing a jumper between the common node and the X1 solder pad doubles the time between refresh cycles.

Power Up Address - This jumper is not needed in standard Cromemco systems. The power up address is factory set to C000h. This set of jumpers allows the address at which execution starts to be changed.

Installation

Turn off all power to the system and unplug it before installing or removing any circuit board.

The DPU is independent of all other boards and may be installed in any available bus slot. No cables are connected to the DPU.

MEMORY SUPPORT

The DPU supports both vertical and horizontal memory configurations.

Horizontal memory, arranged in banks, is used by the 8-bit Cromix Operating System. This memory configuration allows the operating system contained in one 64 Kbyte bank to select one of up to six banks of 64 Kbytes each. This provides a total of 448 Kbytes of addressable memory. Horizontal memory requires the use of Cromemco 64KZ memory boards and does not support the D-series Cromix Operating System. CDOS and the 8-bit Cromix Operating System are supported by horizontal memory configurations.

Vertical memory is used by the D-series Cromix Operating System. This memory configuration allows the operating system to directly address up to 16 Mbytes of memory without the use of bank selection techniques. Vertical memory requires the use of Cromemco MSU series boards together with an MCU. CDOS is not supported by vertical memory configurations. All Cromemco I/O boards are compatible with a DPU configured with vertical memory except the SDI/48KTP and the original WDI. Refer to the sections of this chapter entitled **Using a DPU in a Hard Disk System** and **Using a DPU with an SDI/48KTP.**

Vertical and Horizontal memory cannot be combined within a single system. DO NOT use 64KZ boards in the same system with MSU series boards.

INPUT AND OUTPUT

While in the Z-80A mode of operation, the DPU performs input and output functions by executing Z-80 **in** and **out** instructions which specify the desired values and ports.

While in the MC68000 mode of operation, the DPU performs input and output functions by reading and writing from and to the top bytes of memory (i.e., FFFF00h - FFFFFFh). This area of memory is mapped by the DPU firmware to correspond to ports 0 - FFh.

In both modes of operation, port FFh is reserved for switching from one microprocessor to the other. Refer to the following section for an example of I/O using each microprocessor.

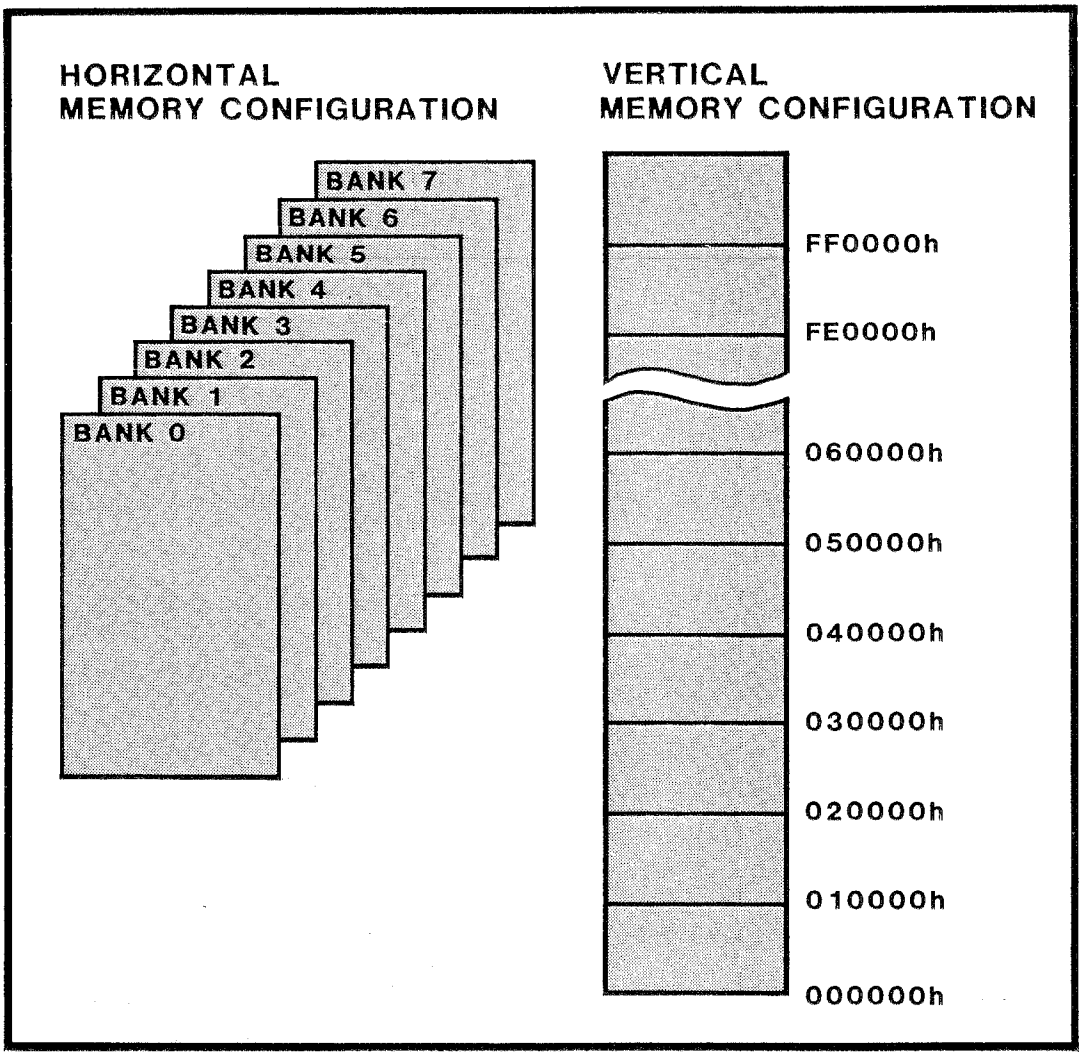

Figure 2-2: MEMORY CONFIGURATIONS

MICROPROCESSOR SELECTION

The DPU board automatically starts up in the Z-80A mode of operation. When a 1 is output to port FFh, the DPU switches to the MC68000 mode of operation.

The first time the MC68000 is used after the power is turned on or the computer is reset, the MC68000 obtains its stack pointer (sp) from location 0 and its program counter (pc) from location 4. Subsequently, when control is switched from the Z-80A to the MC68000, the program continues execution as though it had not been interrupted.

The following Z-80 instructions initiate MC68000 operation with the stack at 6000h and a starting address of 7000h. On subsequent calls to the MC68000, only the two instructions with the comment **switch control to the MC68000** are needed because the stack pointer and program counter have already been established.

```
        ld      hl,intdat           ; initialize sp & pc
        ld      de,0                ;    /
        ld      bc,8                ;   /
        ldir                        ;  /
        ;
        ld      a,1                 ; switch control to
        out     0ffh,a              ; MC68000
        ;
intdat: db      0, 0, 60h, 0        ; location of stack
        db      0, 0, 70h, 0        ; starting address
```

To switch from the MC68000 mode of operation to the Z-80A mode, output a **0** to port FFh. This may be done by writing to the top 64K of memory as follows.

```
    move.b      #0,0ffffffh
```

The 24-bit address to which the zero is moved may be thought of in three segments. The first **ff** indicates that the top 64K of memory is to be used. This is the area of memory which has been reserved for memory mapped I/O. The second **ff** is mandatory. The last **ff** is the port address.

CPU SELECTION IN A HARD DISK SYSTEM

The WDI-II, as received from the factory, is ready for use in a system using a ZPU central processor. The CPU selection circuit traces can be cut and new jumpers installed for the DPU. The jumper locations for each CPU are shown in Figure 2-3. Refer to the following section entitled **Using a DPU in a Hard Disk System.**

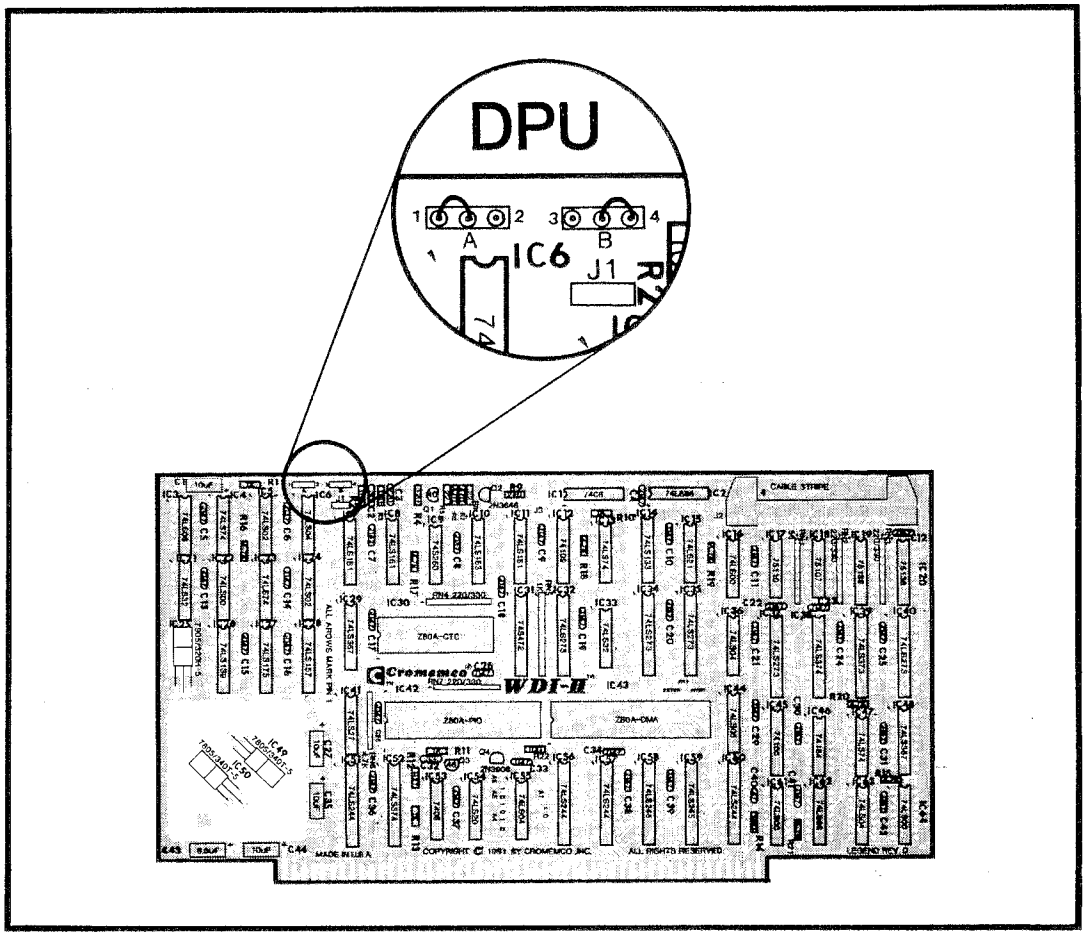

Figure 2-3: WDI-II DPU SELECTION IN A HARD DISK SYSTEM

USING A DPU IN A HARD DISK SYSTEM

The DPU is not compatible with the WDI hard disk interface board.

The WDI-II revision B boards require modification for proper operation with the DPU.

All WDI-II boards require proper CPU jumper selection for use with a DPU. This selection is made at the factory when the DPU comes installed in a system. When the WDI-II is received separately, verify that the DPU central processor has been selected. Refer to Figure 2-3.

WARNING

Use of a WDI, an unmodified WDI-II revision B, or an improperly jumpered WDI-II with a DPU may result in loss of data from the hard disk. Verify proper operation of the hard disk as described in Step 17 below before proceeding.

The following modifications should only be made by your authorized Cromemco dealer or service facility. These modifications are to be made only to WDI-II revision B boards. Figures 2-4a and 2-4b show the required modifications.

1. Turn off the system power and unplug the system. If the board is installed in a system, remove it.

2. Remove the nut and insulating screw which secure IC25. Bend IC25 until it is perpendicular to the board.

3. Place the board on the work area with the component side up.

4. Cut pins 2, 5, 6, and 7 of IC26, and pin 2 of IC6, as near to the board as is possible. Bend the pins out and up until they are parallel to the board surface.

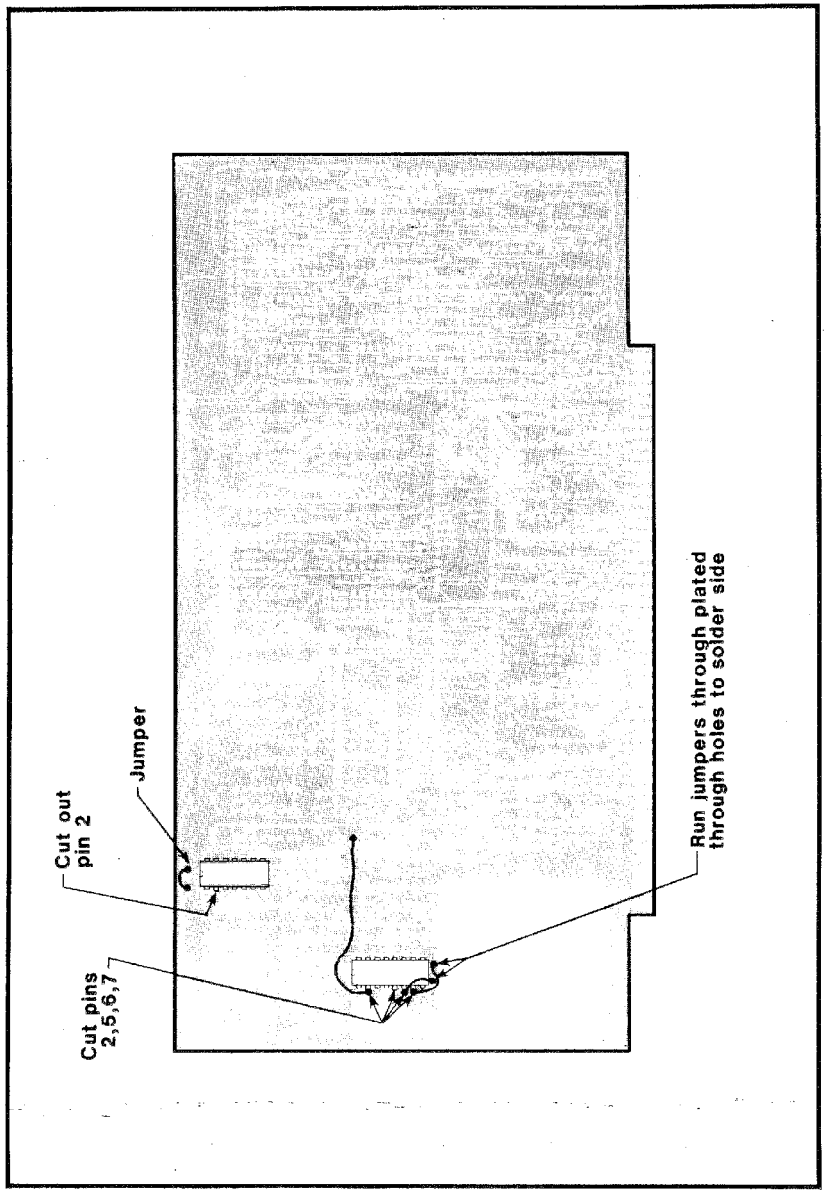

Figure 2-4a: WDI-II MODIFICATIONS - COMPONENT SIDE

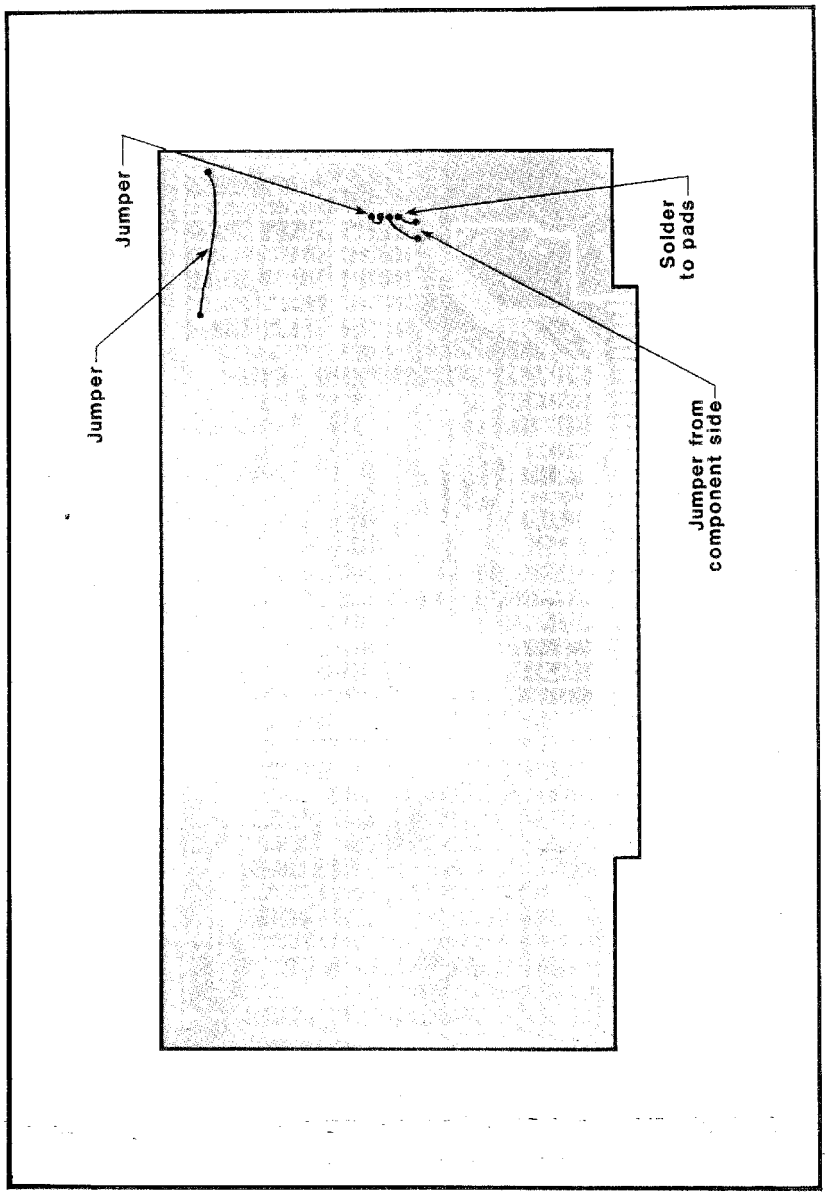

Figure 2-4b: WDI-II MODIFICATIONS - SOLDER SIDE

5. Solder a 2-inch insulated jumper wire to pin 7 of IC26. Feed the jumper wire through the hole near the bottom right side of IC26.

6. Solder a 2-inch insulated jumper wire to pin 6 of IC26. Feed the jumper wire through the hole near the bottom left side of IC26.

7. Turn the board over so that the component side is down. Solder the jumper from pin 7 of IC26 to the board at the solder pad which was connected to pin 6 of IC26.

8. Solder the jumper from pin 6 of IC26 to the board at the solder pad which was connected to pin 7 of IC26.

9. Solder a bare jumper wire between pins 4 and 5 of IC26. Make sure that the jumper **is not shorted** to the trace that passes between pins 4 and 5.

10. Solder an insulated jumper wire between the solder pads of pin 2 of IC6 and pin 3 of IC3.

11. Turn the board over so that the component side is up. Solder an insulated jumper wire between pin 2 of IC26 and pin 3 of IC29.

12. Bend IC25 back to its original position. Secure IC25 with the nut and insulating screw which were removed in Step 2.

13. Verify that the CPU selection jumper is in the ZPU position. The jumper is at the top of IC6 in the form of a circuit trace on the circuit side of the board. If the board has been previously jumpered, it may be necessary to remove the existing jumper and install a new jumper in the ZPU position.

14. Install the WDI-II in the system. Attach the hard disk drive cable to connector J2.

15. Plug the system in and turn on the power.

16. Boot the system using a floppy disk. DO NOT access the hard disk at this time. If you are using a Cromix system, do not boot up on the hard disk and do not mount the hard disk until you have verified that it is operating properly.

17. When using the Cromix Operating System, use the Dump utility to verify proper hard disk operation. Enter the following command (with the hard disk still not mounted). Substitute **hd1** or **hd2** for **hd0** as appropriate.

    dump /dev/hd0

    When using CDOS, use the Dir utility to verify proper hard disk operation. Enter the following command. Substitute **f** or **g** for **e** as appropriate.

    dir e:

18. If the dump is normal and there are no hard disk error messages displayed, the hard disk is operating properly and it may be mounted or established as the root device.

    If error messages are displayed, check all cables and then check all modifications. Do not mount the hard disk until it can be dumped without any error messages being displayed.

USING A DPU WITH AN SDI/48KTP

The D-series Cromix Operating System and the MCU/MSU boards will not support an SDI graphics system.

The DPU may be used with CDOS or an 8-bit Cromix system incorporating 64KZ memory boards in conjunction with an SDI graphics system.

Chapter 3

THE MCU MEMORY CONTROL UNIT

INTRODUCTION

The MCU Memory Control Unit performs three functions in a DPU based system. The MCU controls DPU access to MSU memory boards, provides the operating system with information about errors discovered by the error detection circuits, and corrects single-bit errors.

A modified Hamming algorithm is used for error detection and correction. This method can detect and correct single-bit errors and can detect double-bit errors. Error logging data indicates the MSU board on which each error occurred, the chip row, and, for single-bit errors, the chip column. Error logging provides an early indication of impending memory problems and the necessary information for quick service, should it be required.

Table 3-1 shows the operational specifications for the MCU board.

Table 3-1: MCU SPECIFICATIONS

Support Capacity:	Up to two MSU memory storage boards.
Addressable Memory Locations:	16 megabytes
Buses:	Directly compatible with S-100/IEEE-696. The **M** bus connects MCU and MSU boards.
Power Requirements:	+8 volts @ 1.5 amps
Operating Environment:	0 to 55 degrees C

SETUP AND INSTALLATION

Switch Settings

There are no switches on the MCU.

Jumper Selectable Options

The Cromemco MCU board is ready to be used in your Cromemco system as it is shipped from the factory. There is one set of jumpers which may be used to change the I/O address for experimental purposes. The location of this jumper is shown in Figure 3-1.

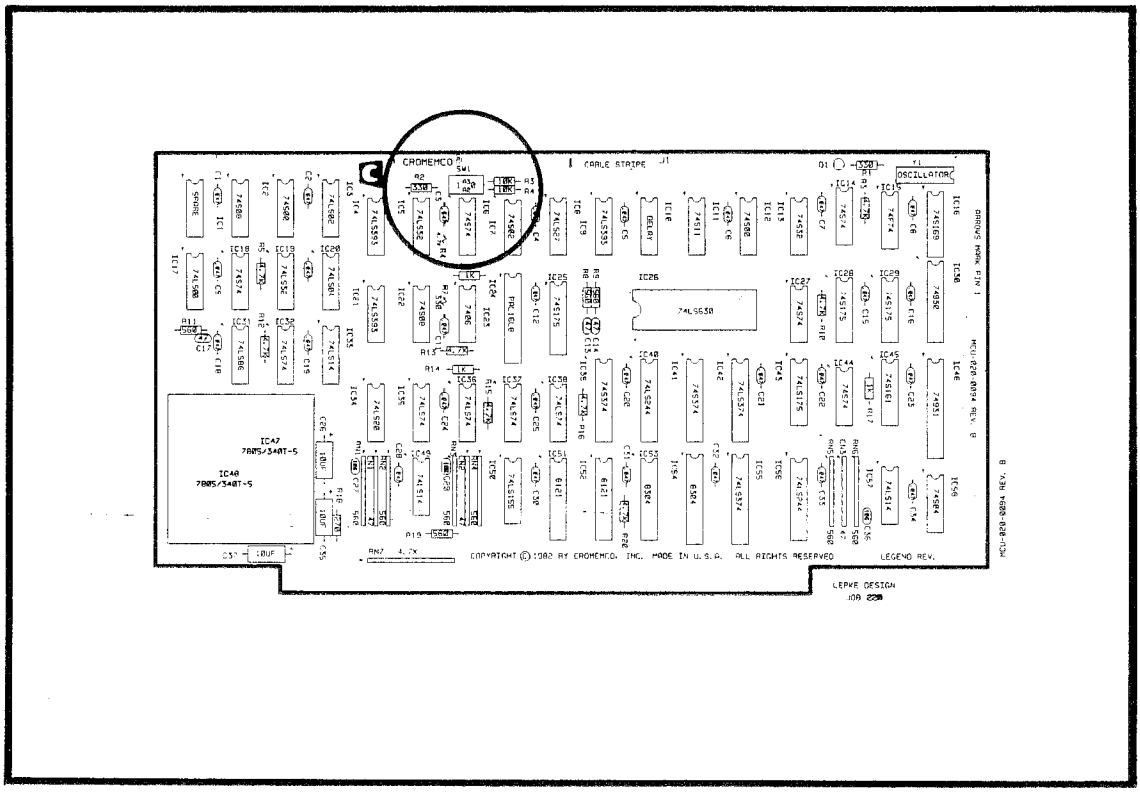

Figure 3-1: MCU JUMPER LOCATION

Installation

Please refer to Chapter 4 for installation information.

ERROR DETECTION AND LOGGING

Please refer to **I/O Port Characteristics** in Chapter 5 while reading this section.

An error is reported by bit D7 of the Control Read byte and the red LED on the MCU board. After the error has been logged by the operating system, this bit may be cleared and the light turned off by the Clear Error command. Error correction will continue regardless of the state of this bit.

Note: When the system is first turned on, the Error Status bit is set which turns the red LED on. The bit should immediately be cleared by sending the Clear Error byte (all zeros) to port 45h Out.

Determining the chip which caused the error is a three step process. The MSU board, the chip row, and the chip column must be identified. Refer to Figure 3-2.

The **MSU ID** byte identifies the board on which the error occurred. Convert the MSU ID byte to binary and match, from left to right, the switch settings on the MSU boards. The 512MSUs have only five switch bits to match while the 256MSUs have six. An MSU ID byte containing zeroes in the five (512MSU) or six (256MSU) most significant binary positions indicate the MSU board addressed at zero. Refer to Table 4-2 for a list of binary values of switches for boards at different memory locations.

The **Chip Row ID** bits identify the row in which the error occurred. Refer to Table 3-2.

Table 3-2: MEMORY ERROR LOCATION BY CHIP ROW

Chip Row ID	Status Bits D5*	Status Bits D4
0	0	0
1	0	1
2	1	0
3	1	1

*Ignore D5 and rows 2 and 3 when MSU ID byte indicates error on 256MSU.

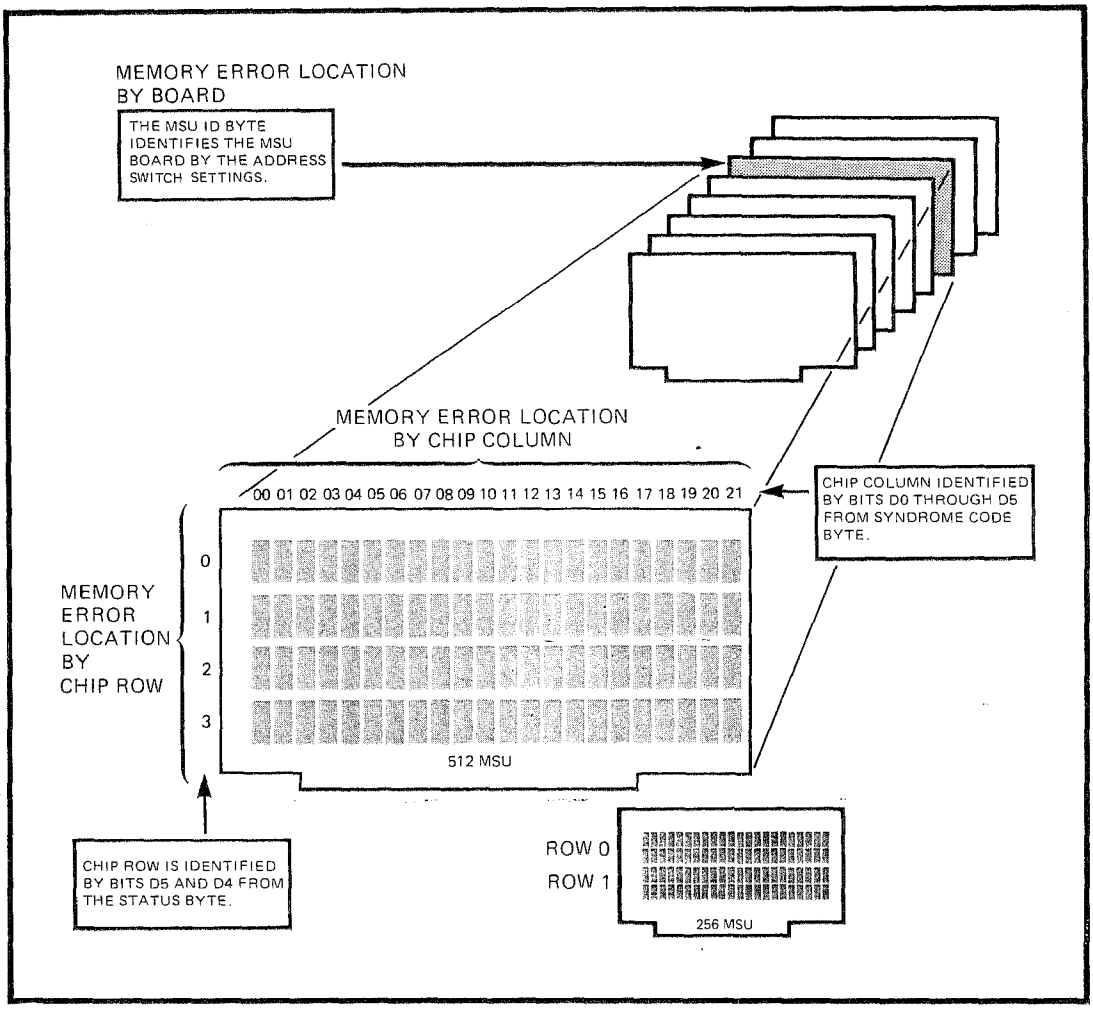

Figure 3-2: MEMORY ERROR LOCATION BY BOARD, CHIP ROW, AND CHIP COLUMN

Table 3-3: MEMORY ERROR LOCATION BY CHIP COLUMN

Chip Column	Syndrome Code Bits					
	D5	D4	D3	D2	D1	D0
00	1	1	0	1	0	0
01	1	1	0	0	1	0
02	1	1	0	0	0	1
03	1	0	1	1	0	0
04	1	0	1	0	1	0
05	1	0	1	0	0	1
06	1	0	0	1	0	1
07	1	0	0	0	1	1
08	0	1	1	1	0	0
09	0	1	1	0	1	0
10	0	1	0	1	1	0
11	0	1	0	1	0	1
12	0	1	0	0	1	1
13	0	0	1	1	1	0
14	0	0	1	1	0	1
15	0	0	1	0	1	1
16	1	1	1	1	1	0
17	1	1	1	1	0	1
18	1	1	1	0	1	1
19	1	1	0	1	1	1
20	1	0	1	1	1	1
21	0	1	1	1	1	1

The **Syndrome Code Data** bits identify the column in which the error occurred. Refer to Table 3-3. The Syndrome Code is only valid for single-bit errors.

Chapter 4

THE MSU MEMORY STORAGE UNIT

INTRODUCTION

Cromemco manufactures two types of MSU boards, each with a different storage capacity. The 256MSU board has a storage capacity of 256 Kbytes of RAM while the 512MSU has 512 Kbytes. These boards are realized as two (256MSU) and four (512MSU) rows of twenty-two 64 Kbit dynamic RAM chips. Each 16-bit data word has six additional bits associated with it. These bits are used by the MCU for error detection and correction.

Table 4-1: 256MSU/512MSU SPECIFICATIONS

Memory Capacity:	256MSU - 128K words of 22 bits (including 6 error detection bits) 256K bytes 512MSU - 256K words of 22 bits (including 6 error detection bits) 512K bytes
Memory Type:	64K RAM 150 nanosecond access time
Buses:	Directly compatible with S-100/IEEE-696. The **M** bus connects MCU and MSU boards.
Power Requirements:	+8 volts @ 1.5 amps
Operating Environment:	0 to 55 degrees C

SETUP AND INSTALLATION

Switch Settings

All memory address switches on either a single 256MSU or 512MSU board in a system should be set to zero (off). This will address the board at zero. If more than one MSU board is used, the address switches should be set according to Table 4-2. Do not set the switches so that memory overlap occurs.

Table 4-2: MSU SWITCH SETTINGS

Lower Memory Boundary		256MSU Switch Bit	512MSU Switch Bit
hex (0000)	decimal (K)	1 2 3 4 5 6	1 2 3 4 5
00	0	0 0 0 0 0 0	0 0 0 0 0
04	256	0 0 0 0 0 1	
08	512	0 0 0 0 1 0	0 0 0 0 1
0C	768	0 0 0 0 1 1	
10	1024	0 0 0 1 0 0	0 0 0 1 0
14	1280	0 0 0 1 0 1	
18	1536	0 0 0 1 1 0	0 0 0 1 1
1C	1792	0 0 0 1 1 1	
20	2048	0 0 1 0 0 0	0 0 1 0 0
.	.	.	.
.	.	.	.
.	.	.	.
F0	15360	1 1 1 1 0 0	1 1 1 1 0
F4	15616	1 1 1 1 0 1	
F8	15872	1 1 1 1 1 0	1 1 1 1 1 *
FC	16128	1 1 1 1 1 1 *	

*reserved for memory mapped I/O

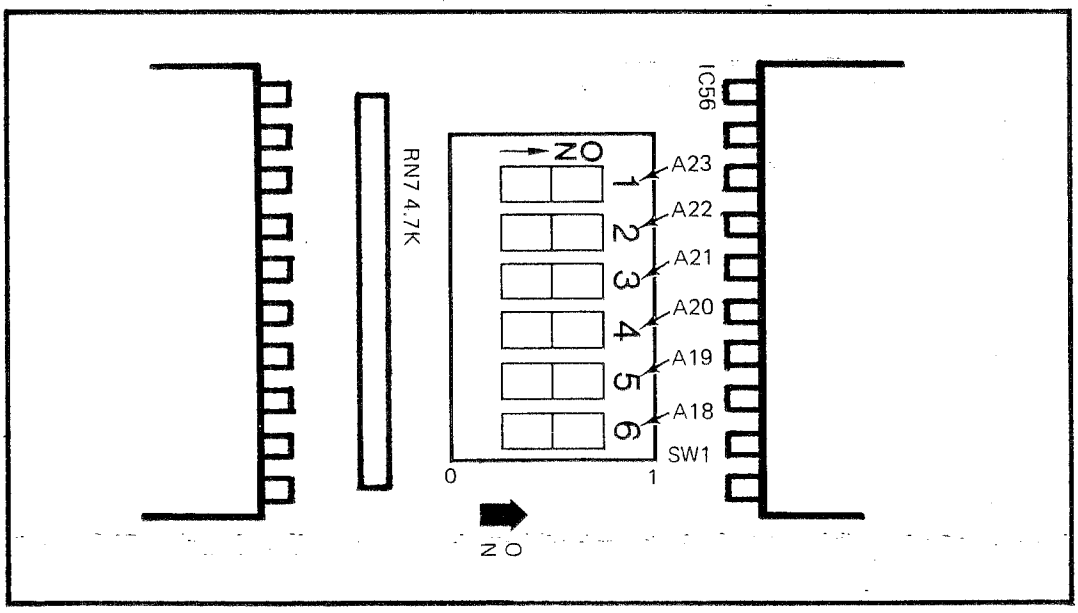

Figure 4-1: 256MSU SWITCH

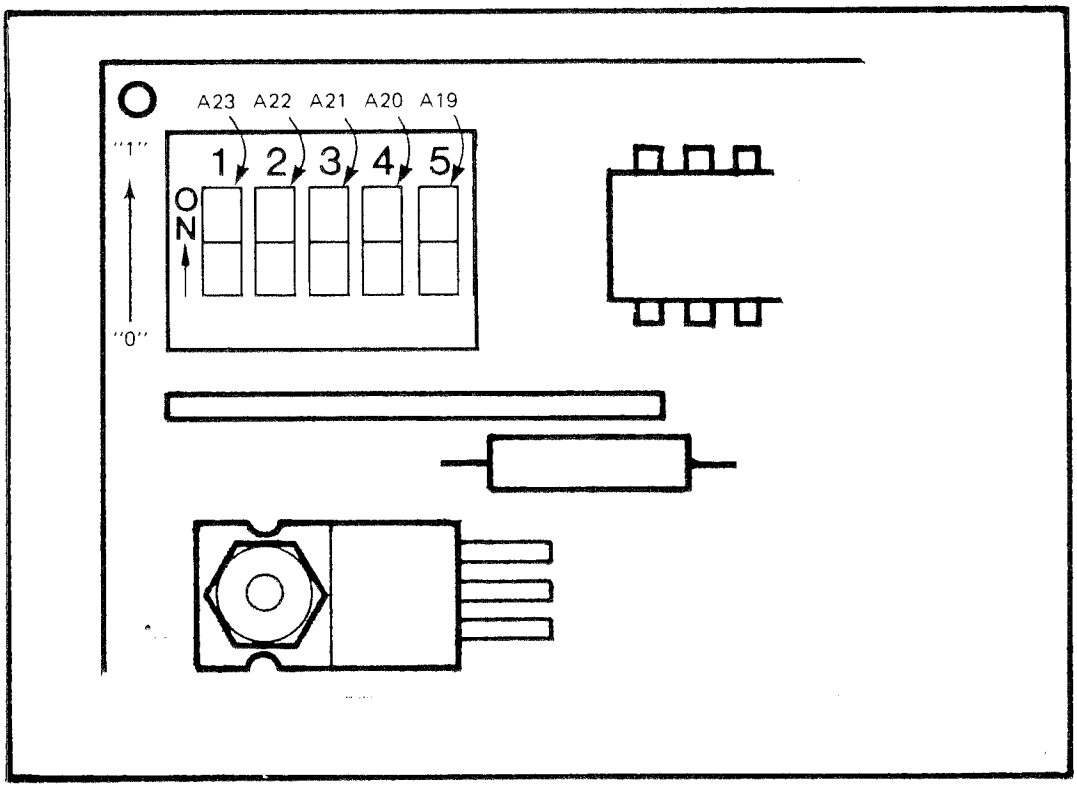

Figure 4-2: 512MSU SWITCH

Jumper Selectable Options

There are no jumper selectable options on either MSU board.

Installation

The MCU and MSU boards share a common cable and therefore must be installed in a physical group. The order or spacing is not important except for the positioning of the overhead M Bus cable.

These boards may be installed as shown in Figure 4-3. When all MCU and MSU boards are installed, take the M bus cable and press it firmly onto the boards as shown in Figure 4-4.

Up to two MSU boards can be used with a single MCU. Cromemco supplies a standard cable (part number 519-0150) with each MCU board for use in systems with one or two MSU boards.

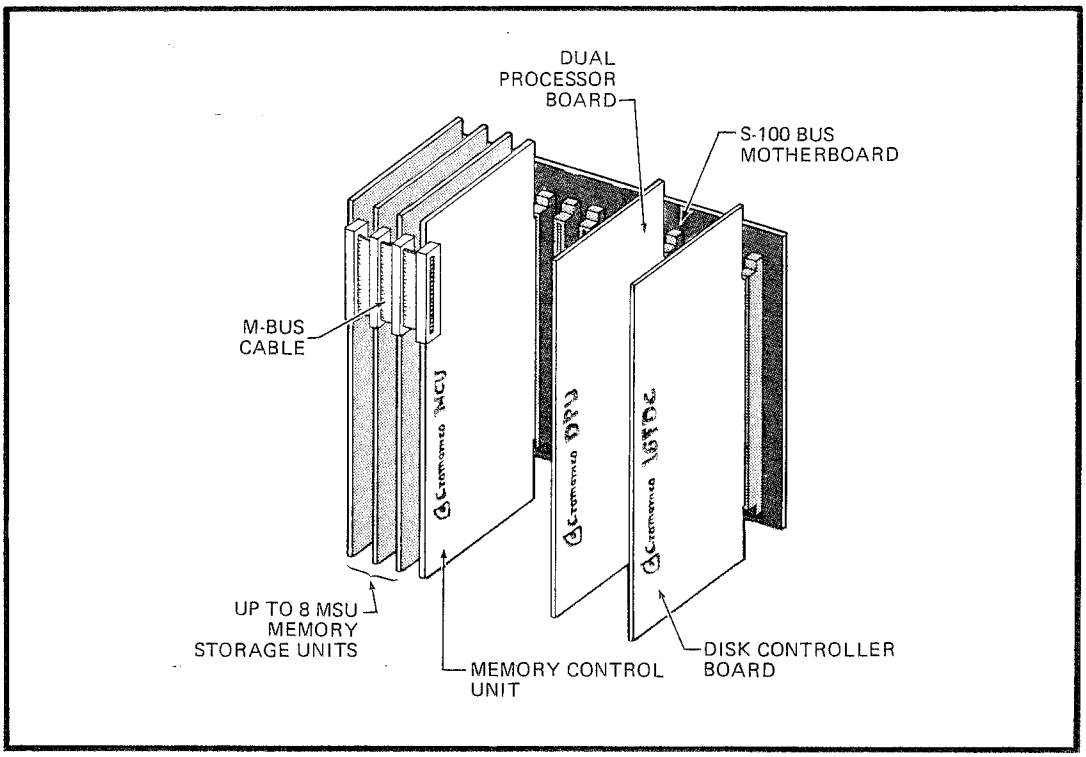

Figure 4-3: DPU, MCU, AND MSU BOARDS INSTALLED IN A STANDARD CROMEMCO SYSTEM

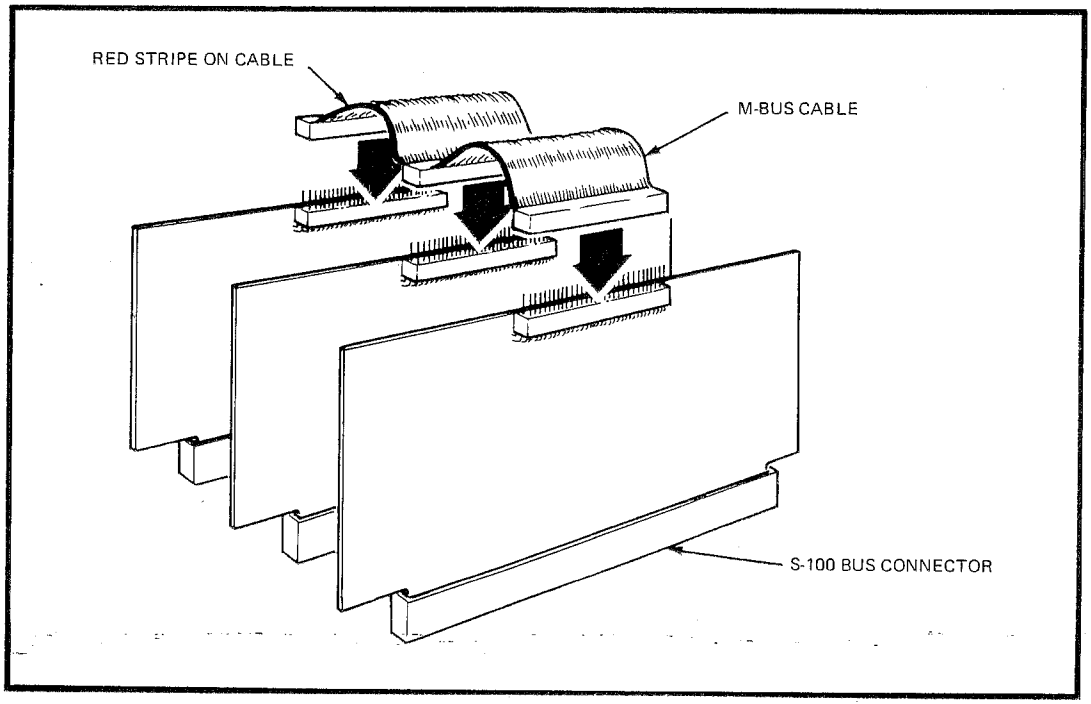

Figure 4-4: INSTALLING THE M BUS CABLE

Chapter 5

BUS SIGNALS AND I/O PORT CHARACTERISTICS

S-100 BUS SIGNALS

The introduction of a new CPU always causes some bus signals to be redefined, some to be deleted, and others to be added. The Z-80A, used in the new DPU central processor, was the heart of the last generation of Cromemco computers. Therefore, the Z-80A, has influenced signal redefinition very little. Major changes have occurred because the DPU uses two microprocessors, one of which is the new MC68000. Most of the new signals concern either board level switching between the two processors, the 16-bit data bus, the 24-bit address bus, or control differences.

The signals of Cromemco's S-100 bus can be grouped into seven functional categories as follows.

1. address
2. control inputs
3. control outputs
4. data
5. DMA data transfer control
6. status
7. utility

Table 5-1 shows each S-100 bus connection, signal mnemonic, name, and function. A bus signal mnemonic not only indicates the signal purpose, but also the active state. Knowing the active state will reveal the logic, binary, and electrical states that are to be expected on a given signal line. When the mnemonic is followed by an **asterisk**, the signal is **active low.** Without the asterisk, the signal is active high. For example, if the signal is GAPK* and the electrical state is low (a more negative voltage), the logic state is true and the binary state is 1. For an active high signal, such as GAPK, an electrical high (more positive voltage) is a logical true and a binary state of 1.

Pin Number	Mnemonic	Signal Name	Function	Pin Number	Mnemonic	Signal Name	Function
1	+8V		U	51	+8V		U
2	+18V		U	52	-18Vur		U
3	XRDY	External Ready	CI	53		undefined	
4		undefined		54	SLVCLR*	Slave Clear	U
5		undefined		55		undefined	
6		undefined		56		undefined	
7		undefined		57		undefined	
8		undefined		58	sXTRQ*	Sixteen Request	S
9		undefined		59	A19	Extended Address Bit 19	A
10		undefined		60	SIXTN*	Sixteen Acknowledge	CI
11		undefined		61	A20	Extended Address Bit 20	A
12	NMI*	Non-maskable Interrupt	CI	62	A21	Extended Address Bit 21	A
13	PWRFAIL*	Power Fail	U	63	A22	Extended Address Bit 22	A
14		undefined		64	A23	Extended Address Bit 23	A
15	A18	Extended Address Bit 18	A	65	MREQ*	Memory Request	U
16	A16	Extended Address Bit 16	A	66	RFSH*	Refresh (Memory)	U
17	A17	Extended Address Bit 17	A	67	MEMDSB*	Memory Disable	U
18	SDSB*	Status Disable	DMA	68	MWRT	Memory Write	S
19	CDSB*	Control Output Disable	DMA	69		undefined	
20		Ground	U	70		Ground	U
21		undefined		71	Z80/68*	Z80/MC68000 Processor Active	CO
22	ADSB*	Address Disable	DMA	72	pRDY	Ready	CI
23	DODSB*	Data Out Disable	DMA	73	pINT*	Interrupt Request	CI
24	ø2	System Clock	U	74	pHOLD*	Hold	CI
25	pSTVAL*	Status Valid Strobe	CO	75	RESET*	Reset (Bus Masters)	U
26	pHLDA	Hold Acknowledge	CO	76	pSYNC	Synchronize	CO
27	EXTAD*	Extended Address Enable	U	77	pWR*	Write	CO
28		undefined		78	pDBIN	Data Bus In	CO
29	A5	Address Bit 5	A	79	A0	Address Bit 0	A
30	A4	Address Bit 4	A	80	A1	Address Bit 1	A
31	A3	Address Bit 3	A	81	A2	Address Bit 2	A
32	A15	Address Bit 15	A	82	A6	Address Bit 6	A
33	A12	Address Bit 12	A	83	A7	Address Bit 7	A
34	A9	Address Bit 9	A	84	A8	Address Bit 8	A
35	DO1/D9	Data Out Bit 1/Data Bit 9	D	85	A13	Address Bit 13	A
36	DO0/D8	Data Out Bit 0/Data Bit 8	D	86	A14	Address Bit 14	A
37	A10	Address Bit 10	A	87	A11	Address Bit 11	A
38	DO4/D12	Data Out Bit 4/Data Bit 12	D	88	DO2/D10	Data Out Bit 2/Data Bit 10	D
39	DO5/D13	Data Out Bit 5/Data Bit 13	D	89	DO3/D11	Data Out Bit 3/Data Bit 11	D
40	DO6/D14	Data Out Bit 6/Data Bit 14	D	90	DO7/D15	Data Out Bit 7/Data Bit 15	D
41	DI2/D2	Data In Bit 2/Data Bit 2	D	91	DI4/D4	Data In Bit 4/Data Bit 4	D
42	DI3/D3	Data In Bit 3/Data Bit 3	D	92	DI5/D5	Data In Bit 5/Data Bit 5	D
43	DI7/D7	Data In Bit 7/Data Bit 7	D	93	DI6/D6	Data In Bit 6/Data Bit 6	D
44	sM1	Status Instruction Fetch	S	94	DI1/D1	Data In Bit 1/Data Bit 1	D
45	sOUT	Status Output	S	95	DI0/D0	Data In Bit 0/Data Bit 0	D
46	sINP	Status Input	S	96	sINTA	Status Interrupt Acknowledge	S
47	sMEMR	Status Memory Read	S	97	sWO	Status Write Out	S
48	sHLTA	Status Halt Acknowledge	S	98	ERROR*	Error	U
49	CLOCK	Clock, 2 MHz	U	99	POC*	Power On Clear	U
50		Ground	U	100		Ground	U

Signal Function Categories: A=address, CI=control inputs, CO=control outputs, D=data, DMA=control for DMA data transfers, S=status, and U=utility.

Table 5-1: S-100 BUS/DPU SIGNALS

S-100 BUS/DPU SIGNAL DEFINITIONS

The following list provides detailed definitions of each S-100 bus signal. Additional information about signal interaction with other boards may be obtained by consulting the appropriate board reference manual.

Address Bus Signals

The address bus, consisting of parallel signal paths of 24 bits, selects specific memory locations or I/O ports. The MC68000 drives all 24 bits directly. During Z-80A operation, the Z-80A drives the lower 16 bits and an auxiliary latch drives the upper 8. On power up or reset, the auxiliary latch is reset.

Memory Addressing - Memory addressing uses 24 bits, **A0 through A23**, providing a 16 Mbyte address range.

I/O Addressing - I/O addressing uses 8 bits, **A0 through A7**, allowing 1 of 256 ports to be selected.

Control Input Signals

DPU control input signals are output by bus slaves such as peripheral interface boards and memory boards. These signals synchronize the operation of the DPU and a bus slave.

External Ready - The **XRDY** signal synchronizes the response of a bus master to a bus slave. It can start and stop DPU operation.

Hold or Bus Request - The **pHOLD*** signal is a DMA bus request generated by the DMA controller of a bus slave. The CPU determines when the request shall be granted and, at the appropriate time, outputs the pHLDA signal.

Interrupt Request - The **pINT*** signal is initiated by a bus slave. Each board may output an interrupt request on this signal line connected to the DPU. The interrupts are serviced according to priorities established by the software and/or hardware.

Non-Maskable Interrupt Request - In a manner similar to pINT*, the **NMI*** signal is initiated by a bus slave. The difference between the signals is that NMI* cannot be masked by software and must be serviced by the DPU as soon as possible.

Ready - The **pRDY** signal is active during normal microprocessor operation. The negation of pRDY is the wait-state request which indicates that an addressed memory board or peripheral is not ready for data transfer.

Sixteen Acknowledge - The **SIXTN*** signal indicates that a request for 16-bit data transfer has been granted and that the transfer may begin. Refer also to the sXTRQ* status signal.

Control Output Signals

The control output signals are output by the DPU to control data transfer and provide the required timing reference.

Data Bus Input Strobe - The **pDBIN** read signal strobes data from the addressed slave onto the data bus.

Hold Acknowledge - The **pHLDA** signal indicates to the board with the highest priority bus request that the DPU has relinquished control of the system bus and that DMA controlled data transfer may begin. Refer to the DMA control signals and pHOLD*.

Processor Active - The **Z-80A/MC68000*** signal indicates which microprocessor is controlling the bus. When high, the Z-80A is in control; when low, the MC68000 is in control.

Status Valid Strobe - The **pSTVAL*** signal indicates that the address and status signals present on the bus are stable and valid. Refer to pSYNC and the status signals.

Synchronization - The **pSYNC** signal indicates the start of a new bus cycle. Refer to pSTVAL* and the status signals.

Write - The **pWR*** write signal strobes data from the data bus to the addressed slave.

Data Bus Signals

The data bus consists of 16 parallel data lines.

Under the control of the Z-80A, the bus is used as two unidirectional 8-line data buses. The data input lines,

DI0 through DI7, bring data to the DPU while the data output lines, **DO0 through DO7,** transfer data from the DPU.

Under the control of the MC68000, all 16 lines, **D0 through D15,** are used as a bidirectional data bus. Refer also to sXTRQ*, SIXTN*, and the control output signals.

DMA Control Signals

The pHOLD* signal is issued by a board when it requires control of the bus for DMA. The DPU acknowledges pHOLD* with a pHLDA signal when it is ready to relinquish control of the bus. At the same time, the following signals disable the CPU bus buffers, effectively isolating the CPU from the bus and allowing the DMA controller to become the bus master.

1. Address Disable **ADSB***
2. Control Output Disable **CDSB***
3. Data Output Disable **DODSB***
4. Status Disable **SDSB***

Status Signals

The following status signals identify the bus cycle in progress and indicate the purpose of the address currently on the bus.

1. Memory read **sMEMR**
2. Operating Instruction Code Fetch **sM1**
3. Input **sINP**
4. Output **sOUT**
5 Memory Write **MWRT**
6. Write cycle **sWO***
7. Interrupt Acknowledge **sINTA**
8. Halt Acknowledge **sHLTA**
9. Sixteen bit data bus request **sXTRQ***

The status signals are best defined in terms of the bus cycle each represents. Table 5-2 shows the electrical state of the status signal for each bus cycle.

Table 5-2: STATUS SIGNAL STATES

Status Signal	Bus Cycle Type						
	Memory Read	Op Code Fetch	Memory Write	Output	Input	Interrupt Acknowledge	Halt Acknowledge
sMEMR	H	H	L	L	L	L	X
SM1	L	H	L	L	L	X	X
sWO*	H	H	L	L	H	H	H
sOUT	L	L	L	H	L	L	L
MWRT	L	L	H	L	L	L	L
sINP	L	L	L	L	H	L	L
sINTA	L	L	L	L	L	H	L
sHLTA	L	L	L	L	L	L	H
sXTRQ*(8-bit)	H	H	H	H	H	H	X
sXTRQ*(16-bit)	L	L	L	L	L	L	X

Utility Signals

Utility signals are necessary to the overall operation of the system. They include power supply and power supply status signals, the system clock, and generalized reset and error signals.

+8 Volts Unregulated - This is the only supply voltage required for the DPU, MCU, and MSU boards. The +18 and -18 Volts Unregulated lines are available for other boards. Regulation of the supply voltage is performed on each board.

Grounds - Signal grounds are connected together on the S-100/IEEE-696 bus.

Phase 2 System Clock - The DPU generates the 0 2 4 MHz system clock signal.

Clock - The 2 MHz **CLOCK** signal is independent of all other bus timing signals. It may be used by circuits to generate time periods or other functions requiring a fixed input frequency.

Reset - The **RESET*** signal resets all bus masters and slaves including the DPU.

Slave Clear - The **SLAVE CLR*** signal resets those bus slaves which monitor this signal.

Power-On Clear - The **POC*** signal is active only at the time that power is applied to the system. When active, POC* issues the RESET* and SLAVE CLR* signals.

Memory Disable - The **MEMDSB*** signal inhibits operation of those memory boards capable of responding to this signal. Operation of Cromemco 64KZ boards will be inhibited by this signal while MSU boards will not be affected.

Memory Request - The **MREQ*** signal indicates that the address on the bus is valid for a memory read or write function.

Refresh - The **RFSH*** signal indicates when the Z-80A is performing a refresh cycle.

M BUS SIGNAL DEFINITIONS

The **M** bus, along with the S-100 bus, provides parallel connections between the MCU and MSU boards. Control, refresh addresses, data, and utility signals are sent from the MCU to the MSU boards. Status and data signals are returned to the MCU by the MSU boards. Table 5-3 lists each **M** bus signal and indicates its function.

The following list provides detailed definitions of each **M** bus signal.

Address and Data Signals

Refresh Address Lines - The MCU places the refresh address on the **RFSH A0** through **RFSH A7** lines. Refer to the RFSH signal.

RAM Data - The **RD0 through RD15** data lines are bidirectional. Data is transferred between the S-100 bus and MSU boards via the MCU board and the M bus. Refer to the EN DIAG DATA* and EN RAM DATA* signals.

Check Bit Data - The data on the **CHECK BIT 0 through CHECK BIT** 5 data lines is calculated from a 16-bit data word being written to memory. The data on these lines is written to the six error detection bits associated with each word in memory. During the memory read cycle, this data is compared to the check bits calculated from the retrieved data word to determine if an error occurred.

Table 5-3: M BUS SIGNALS

Pin Number	Mnemonic	Signal Name	Function
1	GND	Ground	U
2	RFSH A3	Refresh Address Bit 3	A, U
3	RFSH A7	Refresh Address Bit 7	A, U
4	RFSH A2	Refresh Address Bit 2	A, U
5	RFSH A6	Refresh Address Bit 6	A, U
6	RFSH A1	Refresh Address Bit 1	A, U
7	RFSH A5	Refresh Address Bit 5	A, U
8	RFSH A0	Refresh Address Bit 0	A, U
9	RFSH A4	Refresh Address Bit 4	A, U
10	RESET*	Reset	U
11	RD0	Ram Data Bit 0	D
12	RD1	Ram Data Bit 1	D
13	RD2	Ram Data Bit 2	D
14	RD3	Ram Data Bit 3	D
15	RD4	Ram Data Bit 4	D
16	RD5	Ram Data Bit 5	D
17	RD6	Ram Data Bit 6	D
18	RD7	Ram Data Bit 7	D
19	RD15	Ram Data Bit 15	D
20	RD8	Ram Data Bit 8	D
21	RD14	Ram Data Bit 14	D
22	RD9	Ram Data Bit 9	D
23	RD13	Ram Data Bit 13	D
24	RD10	Ram Data Bit 10	D
25	RD12	Ram Data Bit 12	D
26	RD11	Ram Data Bit 11	D
27	MSU SEL*	MSU Select	S
28	+5	+5 Volts	U
29	RFSH	Refresh	U
30	+5	+5 Volts	U
31	COLUMN*	Column Address Enable	C
32	GND	Ground	U
33	ROW*	Row Address Enable	C
34	GND	Ground	U
35	ENRAS*	Enable Row Address Strobe	C
36	GND	Ground	U
37	CAS	Column Address Strobe	C
38	GND	Ground	U
39	ENRAM DATA*	Enable Ram Data	C
40	GND	Ground	U
41	WRITE/(READ*)	Write/Read Enable	C
42	GND	Ground	U
43	CHECK BIT 1	Check Bit 1	D
44	CHECK BIT 4	Check Bit 4	D
45	CHECK BIT 3	Check Bit 3	D
46	CHECK BIT 5	Check Bit 5	D
47	CHECK BIT 2	Check Bit 2	D
48	CHECK BIT 0	Check Bit 0	D
49	EN DIAG DATA*	Enable Diagnostic Data	C
50	GND	Ground	U

Signal Function Categories: A=address, C=control, D=data, S=status, and U=utility

Control Signals

Reset - The **RESET*** signal is derived from the system reset by the MCU. It is not used.

MSU Select - The **MSU SEL*** status signal is output by the selected MSU board, acknowledging that it has been selected for data transfer.

Refresh - The **RFSH** control signal is output by the MCU during a refresh cycle. This signal causes the refresh address to be placed on the address inputs of the RAM chips and the Row Address Strobes to be issued to all RAM chips on all MSUs simultaneously when the EN RAS* strobe is received.

Column Address Enable - The **COLUMN*** signal enables the buffers for address lines A10 through A17 on the 256MSU and A11 through A18 on the 512MSU. This address is latched into the column address inputs of each memory chip. The column address, along with the row address, selects 1 bit of 64 Kbits.

Row Address Enable - The **ROW*** signal enables the buffers for address lines A2 through A9 on the 256MSU and A3 through A10 on the 512MSU. This address is latched into the row address inputs of each memory chip. The row address, along with the column address, selects 1 bit of 64 Kbits.

Enable Row Address Strobe - The **EN RAS*** strobe causes the chip row address strobe (RAS) to be output to a row of memory chips. Address bit A1 selects 1 row of 2 to be strobed on the 256MSU. Address bits A1 and A2 select 1 row of 4 to be strobed on the 512MSU. In the refresh mode, RFSH selects all chip rows and EN RAS* causes them to be strobed simultaneously. Strobing RAS latches the row address into the RAM chip.

Column Address Strobe - The **CAS** signal asserts the column address strobe of each RAM chip.

Enable RAM Data - The **EN RAM DATA*** signal enables the RAM data bus buffers on the MSU involved in the memory operation.

Write - The **WRITE** signal causes the individual write signals to be issued to the memory chips.

Enable Diagnostic Data - The **EN DIAG DATA*** signal inhibits the RD0 through RD7 buffers and enables the diagnostic ROM.

I/O PORT CHARACTERISTICS

The following is a list of I/O port addresses and their functions.

44h Out: Control

The **Control Write** byte sends control data from the CPU to the MCU.

D7-D2 - These bits must be zero.

D1 Enable Error Detection and Correction (EN EDAC) - This bit enables the error detection and correction circuits on the MCU board.

D0 Enable Diagnostic (EN DIAG) - This bit enables the diagnostic function of the memory system.

44h In: Status

The **CONTROL READ** byte sends status information from the MCU to the CPU.

D7 Error - Indicates that an error has been detected. When this bit is on, the red LED on the MCU will be lit.

D6 Unused - This bit will read as zero.

D5-D4 Chip Row ID - These signals identify the row containing the chip which generated the error. The 256MSU, having only two rows of chips, uses only D4 to identify the row while the 512MSU uses both D5 and D4. Refer to Chapter 3, **Error Logging.**

D3-D2 - not used

D1 Error Circuit Status - This signal indicates that the error detection and correction circuits are enabled.

D0 Diagnostic Circuit Status - This signal indicates that the diagnostic circuits are enabled.

45h In: Syndrome Code

The **Syndrome Read** byte contains information pertinent to an error condition.

D7 Diagnostic Circuit Status at Error - This bit indicates the diagnostic circuits were enabled when the error occurred. A logical false indicates that the error occurred under normal operation.

D6 Error Status - This bit indicates that the error was a single error; a logical false indicates a double error.

D5-D0 Syndrome Code Data - These data bits identify the chip column in which the error occurred. Refer to Chapter 3, **Error Logging.**

45h Out: Clear Error

The **Clear Error** command clears bit D7 of the Control Read status word. This byte should be set to all zeroes.

46h In: MSU ID

The **Error Address READ** byte identifies the MSU board containing the memory chip in which an error occurred. Refer to Chapter 3, **Error Logging.**

46h Out: not used

47h In: not used

47h Out: not used

FFh Out: MC68000/Z-80A Switch

The **MC68000/Z-80A Switch Output Byte** enables either the MC68000 or the Z-80A microprocessor on the DPU. When one is enabled, the other is disabled. Refer to Chapter 2, **Microprocessor Selection.**

D7-D1 - not used

D0 Microprocessor Selection Switch - When set, this bit turns the MC68000 on. When reset, it turns the Z-80A on.

INTERRUPT VECTOR TRANSLATION

The interrupt vectors supplied by system devices must be translated into vectors that can be properly interpreted by the MC68000. The following equation shows the mathematical relationship between the device vector and the vector that is received by the MC68000. After translation, all device generated vectors fall within the user interrupt area of the MC68000 vector table.

$$Vh_{68000} = INT\ (Vh_{DEVICE}/2) + 40h$$

Where:

Vh_{68000} = the hexadecimal equivalent of the binary vector input to the MC68000,

INT = the integer (whole number without the fraction) of the portion of the equation within the parentheses,

Vh_{DEVICE} = the hexadecimal vector output by the board or device within the system,

40h = hexadecimal 40.

The following table shows vector translation examples.

If Vh_{DEVICE} is	then Vh_{68000} is
0h or 1h	40h
Ch or Dh	46h
7Eh or 7Fh	7Fh
FEh or FFh	BFh

Appendix A

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1. Your name, address and telephone number,
2. the return authorization number,
3. a description of the problem, and
4. proof of the date of retail purchase.

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Other Important Provisions:

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