

Cromemco
ZPU
Instruction
Manual

Five Dollars

CROMEMCO

ZPU

Instruction Manual

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ZPU INSTRUCTION MANUAL

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Section 1

INTRODUCTION

This manual contains assembly and operating instructions for Cromemco's powerful 4 MHz S-100 bus compatible Z-80A CPU card (ZPU). The ZPU is designed to bring the power and speed of the Z-80A processor to systems using the 8080-oriented S-100 bus. Thus, the manual also includes an extensive section detailing S-100 bus features.

Read Section 2, OPERATING INSTRUCTIONS, before inserting the ZPU into your system S-100 bus.

TECHNICAL SPECIFICATIONS

Z-80A Microprocessor Card

PROCESSOR: 4 MHz version of the Z-80.

CLOCK RATE: 2/4 MHz (switch selectable).

INSTRUCTION SET: 158 instructions including the 78 instructions of the 8080.

POWER-ON JUMP: jumper wire enabled.

POWER-ON JUMP LOCATIONS:
16 locations switch selectable.

WAIT STATE GENERATION:

0 - 4 wait states jumper wire selectable.

M1 WAIT STATE: jumper wire selectable.

BUS: S-100.

POWER REQUIREMENTS: +8 volts @
1.1 A.

OPERATING ENVIRONMENT: 0 - 55°C.

SECTION 2

OPERATING INSTRUCTIONS

The Cromemco ZPU is an S-100 bus compatible CPU (Central Processing Unit) which uses the powerful Z-80A microprocessor. The Cromemco ZPU has an exclusive set of features designed to increase your total system computing power. Most importantly, the ZPU operates reliably at a 4 MHz clock rate--twice the speed of most other microcomputer systems. The ZPU offers Power-On Jump capability, an on-board wait state generator, optional independent selection of M1 wait states, address mirroring circuitry, and several other features discussed in this section.

2.1 POWER-ON JUMP

The ZPU Power-On Jump circuitry allows the board to be used in an S-100 bus system without front panel controls (e.g., Cromemco's Z-2, Z-2D and SYSTEM THREE). When system power is turned ON, the ZPU hardware forces and automatic jump to one-of-sixteen memory location selected with the four position Jump Address select switch.

The automatic jump address corresponding to each switch setting is tabulated below:

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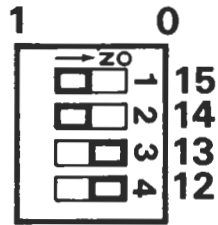
| <u>SWITCH</u> | | | | <u>POWER-ON</u> |
|---------------|------------|------------|------------|---------------------|
| <u>A15</u> | <u>A14</u> | <u>A13</u> | <u>A12</u> | <u>JUMP ADDRESS</u> |
| 0 | 0 | 0 | 0 | 0000H |
| 0 | 0 | 0 | 1 | 1000H |
| 0 | 0 | 1 | 0 | 2000H |
| 0 | 0 | 1 | 1 | 3000H |
| 0 | 1 | 0 | 0 | 4000H |
| 0 | 1 | 0 | 1 | 5000H |
| 0 | 1 | 1 | 0 | 6000H |
| 0 | 1 | 1 | 1 | 7000H |
| 1 | 0 | 0 | 0 | 8000H |
| 1 | 0 | 0 | 1 | 9000H |
| 1 | 0 | 1 | 0 | A000H |
| 1 | 0 | 1 | 1 | B000H |
| 1 | 1 | 0 | 0 | C000H |
| 1 | 1 | 0 | 1 | D000H |
| 1 | 1 | 1 | 0 | E000H |
| 1 | 1 | 1 | 1 | F000H |

Note the Jump Address switch determines the four highest order bits in the jump address, with all other address bits set to logic 0.

EXAMPLE 1

Suppose you have a Cromemco Z-2D System which comes standard with a 4FDC card and RDOS (Resident Disk Operating System) in PROM memory. This program, which resides at C000-C3FFH, provides a convenient way to start-up a system. To effect an automatic jump to location C000H, the Jump Address switch should be set as shown below:

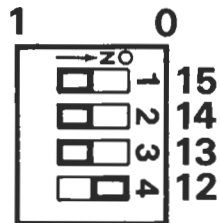
**JUMP
ADDRESS**



EXAMPLE 2

Suppose you have a Cromemco Z-2 System, and you want to force a jump to the Z-80 Monitor program after a system Power-On or RESET. The Z-80 Monitor spans addresses E000-E3FFH, so you would then set the Jump Address switch to E000H as shown below:

**JUMP
ADDRESS**



Your ZPU is factory shipped with the Power-On Jump feature enabled. To disable the function (resulting in an automatic jump to address 0000H only on a Power-On Clear or RESET), carefully cut the foil trace connecting two points on the board labeled "JUMP ENABLE".

If your computer system has RESET and EXAMINE front panel controls, the function of each of these switches is

altered when the automatic jump feature is enabled. Following a system RESET, the first instruction executed is not at address 0000H, but rather at one of the sixteen addresses specified with the Jump Address switch. Immediately after a RESET, the EXAMINE switch must be toggled twice in order to examine the automatic jump location: once to clear the automatic jump and a second time to perform the actual examine operation.

For computers with front panel switches and indicators, you can see how the Power-On Jump works by pressing the STOP switch, then raising the RESET switch. The number C3H should appear in the DATA display. This is the op code of the hardware jump instruction. Now press the EXAMINE NEXT switch; all 0's will appear in the DATA display indicating the low order 8 bits of the jump address. Press the EXAMINE NEXT switch again; the high order 8 bits of the jump address will now appear in the DATA display. The lower four bits will all be 0's, and the higher four bits will display the Jump Address switch bits.

2.2 Z-80A CLOCK FREQUENCY SELECTION

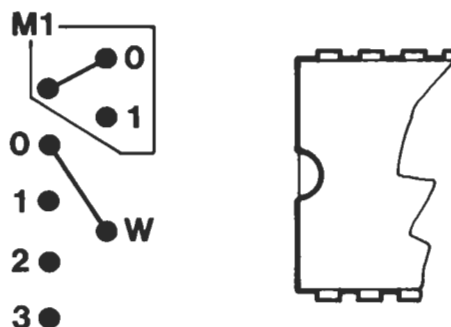
The Z-80A may be clocked at either 4 MHz (with a 250 nsec cycle time) or 2 MHz (with a 500 nsec cycle time). The operating frequency is switch selectable with the toggle switch labeled "2" (2 MHz) and "4" (4 MHz).

The line previously labeled "STACK" on the S-100 bus is used by the ZPU as a 4 MHz indicator line. The Cromemco Z-1 System front panel indicator which monitors this line is labeled "4 MHz" (it may be labeled "STACK" on non-Cromemco products). The indicator will be ON for 4 MHz operation, and OFF for 2 MHz operation.

2.3 WAIT STATE SELECTION

The ZPU features an on-board WAIT STATE generator to match the Z-80A clock frequency to your system's memory access time. The ZPU allows two types of wait state insertion. The first inserts from 0 to 3 wait state cycles (1 cycle = 250 nsec at 4 MHz; 500 nsec at 2 MHz) during every machine cycle; the second type inserts either one or no additional wait states during an instruction fetch cycle only (referred to as an M1-cycle in the Zilog literature), where the timing requirements are the tightest.

If you are using Cromemco memory boards, leave your ZPU in its factory wired condition (no wait states); all wait state selection is done on the memory boards if required. Wait state selection to accomodate other boards is accomplished by re-configuring ZPU board jumpers M1 and W (just to the left of the Z-80A chip).



A jumper wire from "W" to points labeled 0, 1, 2 and 3 selects 0, 1, 2 or 3 wait states on every machine cycle. A jumper wire from "M1" to points labeled 0 and 1 selects either 0 or 1 additional wait states during an M1 cycle. When operating the ZPU at 4 MHz, a 250 nsec memory board requires no wait states to be compatible with the Z-80A CPU. Each additional W-wait state (from one to three) slows the required memory access time by 250 nsec, while an M1-wait state slows the required memory access time an additional 110 nsec (approx.). The corresponding figures for 2 MHz operation are; no wait states for 500 nsec memory boards, 500 nsec per W-wait state added, and an additional 235 nsec (approx.) for an M1-wait state. You may find these figures to be somewhat conservative in actual practice. To get the maximum performance from your memory, you may wish to experimentally find the fewest number of wait states required for reliable operation.

The ZPU comes factory pre-wired for no wait states. If a change is necessary, carefully cut the factory installed foil trace between points labeled "W" and "0", or between

"M1" and "0" as appropriate before installing new jumper wires.

2.4 ADDRESS MIRROR SELECTION

The 8080 microprocessor repeats (or mirrors) the 8-bit address of an I/O port in both the high and low order 8 bits of the address bus. Although this characteristic is not inherent in the Z-80A CPU, the ZPU board is designed to mimic this behavior through address mirror circuitry assuring ZPU compatibility when updating older 8080 systems.

The address mirror circuitry is enabled by the short run of foil between pads labeled "AM" and "ON" (between IC7 and IC8 on the board). If you wish to disable this circuitry, carefully cut the existing foil trace, and in its place, connect pads "AM" and "OFF" with a jumper wire.

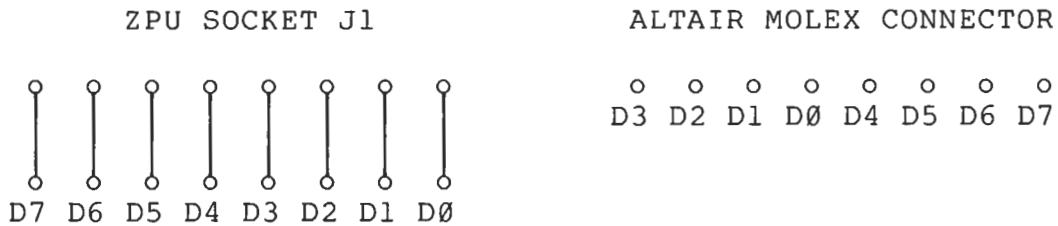
2.5 REFRESH ENABLE

Certain types of dynamic memory boards require that the refresh address supplied by the Z-80A be mirrored in the eight high order address lines. To enable this feature, install a jumper wire between the two pads labeled "RFSH ENAB". The ZPU is factory shipped with this connection broken as no Cromemco memory boards require address mirroring.

2.6 ALTAIR OR IMSAI INSTALLATION

If you are using an IMSAI 8080 computer, the cable from the front panel may be plugged directly into socket J1 on the ZPU board.

If you are using an ALTAIR 8800 or 8800A computer, a DIP plug must be installed in place of the Molex connector on the front panel cord. When wiring the connector, note that the data lines are not arranged sequentially on the ALTAIR connector as they are on the ZPU connector (refer to the figure below for wiring information).



Section 3

THE S-100 BUS

The Cromemco ZPU card is designed to interface the Z-80A microprocessor to the industry standard S-100 bus. The S-100 bus, in turn, is designed to interface a CPU module to as many as 20 additional memory, I/O interface, or other processor modules. This bus standard was originally known as the "Altair" bus appearing in the MITS Altair line of computers in 1975. The bus was quickly adopted by a host of microcomputer manufacturers and was named the "S-100" bus by Dr. Roger Melen of Cromemco Inc. in August of 1976. The S-100, or "Standard-100", bus is now widely regarded as the most-used busing standard ever developed in the computer industry.

Physically, the S-100 bus is realized as a set of 100-contact edge connectors mounted to a common mother board and wired in parallel. The modules that plug into the edge connectors of the S-100 bus are circuit cards that measure 5" by 10".

The S-100 bus was originally designed for use with a CPU module using the 8080 microprocessor, and consequently, the bus signal definitions closely follow those of an 8080 system. The Z-80A microprocessor signal lines differ quite

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dramatically from the 8080 lines (e.g., the Z-80A is driven by a single phase clock, the 8080 by a two phase clock), but the ZPU board is designed to supply all "8080-like" S-100 bus functions (including the two phase clock). The signals of the S-100 bus can be grouped in four functional categories: 1) power supply, 2) address, 3) data, and 4) clock and control signals. A complete listing of the S-100 bus signals is shown below:

S-100 BUS

| | | | |
|---------------------------|----------------|--------------------------|-------------------------|
| 1. +8 VOLTS | 26. pHLDA | 51. +8 VOLTS | 76. pSYNC |
| 2. +18 VOLTS | 27. pWAIT | 52. <u>-18 VOLTS</u> | 77. pWR |
| 3. EXT. READY | 28. pINTE | 53. <u>SSW DISABLE</u> | 78. pDBIN |
| 4. UNDEFINED | 29. A5 | 54. EXT. CLEAR | 79. A0 |
| 5. " | 30. A4 | 55. UNDEFINED | 80. A1 |
| 6. " | 31. A3 | 56. " | 81. A2 |
| 7. " | 32. A15 | 57. " | 82. A6 |
| 8. " | 33. A12 | 58. " | 83. A7 |
| 9. " | 34. A9 | 59. " | 84. A8 |
| 10. " | 35. D01 | 60. " | 85. A13 |
| 11. " | 36. D00 | 61. " | 86. A14 |
| 12. <u>NMI</u> | 37. A10 | 62. " | 87. A11 |
| 13. UNDEFINED | 38. D04 | 63. " | 88. D02 |
| 14. " | 39. D05 | 64. " | 89. D03 |
| 15. " | 40. D06 | 65. <u>MEM. REQUEST</u> | 90. D07 |
| 16. " | 41. DI2 | 66. REFRESH | 91. DI4 |
| 17. " | 42. DI3 | 67. UNDEFINED | 92. DI5 |
| 18. <u>STATUS DISAB.</u> | 43. DI7 | 68. <u>MEM. WRITE</u> | 93. DI6 |
| 19. <u>CONTROL DISAB.</u> | 44. sM1 | 69. <u>PROTECT STAT.</u> | 94. DI1 |
| 20. UNPROT. MEM. | 45. sOUT | 70. PROTECT MEM. | 95. DI0 |
| 21. <u>SINGLE STEP</u> | 46. sINP | 71. RUN | 96. sINTA |
| 22. <u>ADDR. DISAB.</u> | 47. sMEMR | 72. pREADY | 97. sW0 |
| 23. <u>D0 DISABLE</u> | 48. sHLTA | 73. pINT | 98. <u>sSTACK/4 MHz</u> |
| 24. ϕ 2 CLOCK | 49. 2 MHz CLK. | 74. pHOLD | 99. <u>PWR-ON CLEAR</u> |
| 25. ϕ 1 CLOCK | 50. GROUND | 75. pRESET | 100. GROUND |

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S-100 POWER SUPPLY

| | |
|-----------|-----------------|
| +8 Volts | Pins 1 and 51 |
| +18 Volts | Pin 2 |
| -18 Volts | Pin 52 |
| Ground | Pins 50 and 100 |

Three unregulated D.C. power supply voltages appear on the S-100 bus: +8 volts, +18 volts and -18 volts. The main power supplies are unregulated, so power supply regulation must be performed on each individual circuit card, usually by three-terminal regulator IC's.

Distributed power supply regulation has several advantages over a single, centrally regulated supply:

-Each card is individually protected from voltage overload. Faulty regulation in one master supply cannot destroy the entire computer system.

-The heat produced by voltage regulation is thermally distributed through a larger physical volume.

-Voltage drops along the bus do not influence the voltage on the card circuitry itself.

-Initial cost of the computer mainframe is lower. Regulation circuitry is purchased only as additional cards are added to

the system.

An S-100 bus mainframe capable of accepting a full 21 cards (like the Cromemco Z-2, Z-2D and SYSTEM THREE) typically has a power supply current capacity of 30 amps at +8 volts and 15 amps at +18 and -18 volts.

S-100 ADDRESS SIGNALS

| | | | |
|----|--------|-----|--------|
| A0 | PIN 79 | A8 | PIN 84 |
| A1 | PIN 80 | A9 | PIN 34 |
| A2 | PIN 81 | A10 | PIN 37 |
| A3 | PIN 31 | A11 | PIN 87 |
| A4 | PIN 30 | A12 | PIN 33 |
| A5 | PIN 29 | A13 | PIN 85 |
| A6 | PIN 82 | A14 | PIN 86 |
| A7 | PIN 83 | A15 | PIN 32 |

There are 16 address lines on the S-100 bus allowing the direct addressing of 65,536 words of memory space. Tri-state TTL drivers are used to drive the address bus. One S-100 bus control line (ADDRESS DISABLE) can be used to disable the address drivers to allow DMA operations when other cards need to take control of the address bus.

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S-100 DATA SIGNALS

| | | | |
|-----|--------|-----|--------|
| DI0 | PIN 95 | DO0 | PIN 36 |
| DI1 | PIN 94 | DO1 | PIN 35 |
| DI2 | PIN 41 | DO2 | PIN 88 |
| DI3 | PIN 42 | DO3 | PIN 89 |
| DI4 | PIN 91 | DO4 | PIN 38 |
| DI5 | PIN 92 | DO5 | PIN 39 |
| DI6 | PIN 93 | DO6 | PIN 40 |
| DI7 | PIN 43 | DO7 | PIN 90 |

Although the S-100 bus is based on the 8080 microprocessor which has an 8-bit bi-directional data bus, the S-100 has two directional data busses, each 8 bits wide. The data input bus is called the DI bus, and the data output bus is called the DO bus. The S-100 provides for one control line to disable the DO bus (DO DISABLE) for DMA operations.

S-100 CLOCK AND CONTROL SIGNALS

| | | | |
|-----------------------|--------|-----------------------|--------|
| <u>EXT READY</u> | PIN 3 | <u>SSW DISABLE</u> | PIN 53 |
| <u>NMI</u> | PIN 12 | <u>EXT. CLEAR</u> | PIN 54 |
| <u>STATUS DISAB.</u> | PIN 18 | <u>MEM. REQ.</u> | PIN 65 |
| <u>CONTROL DISAB.</u> | PIN 19 | <u>REFRESH</u> | PIN 66 |
| <u>UNPROTECT</u> | PIN 20 | <u>MEM. WRITE</u> | PIN 68 |
| <u>SINGLE STEP</u> | PIN 21 | <u>PROTECT STATUS</u> | PIN 69 |
| <u>ADDR. DISAB.</u> | PIN 22 | <u>PROTECT</u> | PIN 70 |
| <u>DO DISABLE</u> | PIN 23 | <u>RUN</u> | PIN 71 |
| $\phi 2$ | PIN 24 | <u>pREADY</u> | PIN 72 |
| $\phi 1$ | PIN 25 | <u>pINT</u> | PIN 73 |
| <u>PHLDA</u> | PIN 26 | <u>pHOLD</u> | PIN 74 |
| <u>pWAIT</u> | PIN 27 | <u>pRESET</u> | PIN 75 |
| <u>pINTE</u> | PIN 28 | <u>pSYNC</u> | PIN 76 |
| <u>sM1</u> | PIN 44 | <u>pWR</u> | PIN 77 |
| <u>sOUT</u> | PIN 45 | <u>pDBIN</u> | PIN 78 |
| <u>sINP</u> | PIN 46 | <u>sINTA</u> | PIN 96 |
| <u>sMEMR</u> | PIN 47 | <u>sW0</u> | PIN 97 |

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| | | | |
|-------------|--------|--------------|--------|
| sHLTA | PIN 48 | sSTACK/4 Mhz | PIN 98 |
| 2 MHz CLOCK | PIN 49 | PWR-ON CLEAR | PIN 99 |

There are three clock signals on the S-100 bus: $\phi 1$ (pin 25), $\phi 2$ (pin 24) and 2 MHz Clock (pin 49). The 2 MHz CLOCK line is always a 2 MHz signal regardless of the processor clock frequency. $\phi 1$ and $\phi 2$ provide a two phase non-overlapping clocks at the processor clock frequency. All clock and control signals on the S-100 bus are standard TTL levels.

Control signals on the S-100 bus which are functionally equivalent to control signals used with the 8080 microprocessor are prefixed with a lower case "p". Thus pHLDA, pWAIT, pINTE, pREADY, pHOLD, p $\overline{\text{INT}}$, p $\overline{\text{RESET}}$, pSYNC, p $\overline{\text{WR}}$ and pDBIN serve the same function as the corresponding control signals for the 8080 microprocessor. Similarly, S-100 bus signals prefixed with an "s" are functionally equivalent to the corresponding outputs of the 8080 status latch. These signals include sM1, sOUT, sINP, sMEMR, sHLTA, sINTA, s $\overline{\text{WO}}$ and sSTACK. The sSTACK line (pin 98) is used to indicate stack operations in 8080 systems; however in Cromemco Z-80A systems, this line is used instead to indicate 4 MHz operation (logic 1) or 2 MHz operation (logic 0).

Four of the S-100 control lines are dedicated to tri-stating bus drivers (e.g., during DMA operations). ADDRESS

$\overline{\text{DISABLE}}$ is used to disable the address bus; $\overline{\text{DO DISABLE}}$ is used to disable the Data Output bus; $\overline{\text{STATUS DISABLE}}$ is used to disable the status lines (those prefixed with an "s"); and $\overline{\text{CONTROL DISABLE}}$ is used to disable the clock and control signals.

Three of the S-100 control signals shown are used only with the Z-80A CPU. These are $\overline{\text{NMI}}$ (Non-Maskable Interrupt), $\overline{\text{MEMORY REQUEST}}$, and $\overline{\text{REFRESH}}$. The functions of these signals on the S-100 bus are the same as the corresponding lines of the Z-80A microprocessor.

The remaining ten defined lines are used primarily in S-100 systems with an operator's front panel. A front panel switch can be used to protect RAM or PROM memory from accidental memory write operations by issuing a PROTECT (pin 70) signal to the bus. The memory can be unprotected by the UNPROTECT (pin 20) signal, and the current PROTECTED or UNPROTECTED status of any memory can be determined from the PROTECT STATUS (pin 69) signal. MWRITE (pin 68) is used to indicate a memory write operation and is used in conjunction with front panel memory deposit. EXT. READY is an alternate to pREADY to avoid bus conflicts when both front panel circuitry and other circuitry need control of the processor READY line.

Front panel controls can be used to run or stop the

processor or to single step through a program as indicated on the RUN (pin 71) line and the SINGLE STEP (pin 21) line. When front panel sense switches are assigned to a specific input port, the SENSE SWITCH DISABLE ($\overline{\text{SSW DISABLE}}$, pin 53) is used to disable the DI bus during sense switch inputs. $\overline{\text{EXTERNAL CLEAR}}$ (pin 54) is activated by an auxillary front panel switch, but it is assigned to no specific function. Finally, there is the $\overline{\text{POWER-ON CLEAR}}$ signal that remains at logic 0 when power is first turned on, and then transitions to logic 1 approximately 100 milliseconds later to indicate that power is on and the power supply voltages have stabilized.

Section 4

ASSEMBLY INSTRUCTIONS

If you purchased a ZPU kit, you will find assembly to be straight-forward provided you follow the instructions below. All parts are inserted from the component side of the board (with the white printed legend), and all soldering is done from the opposite side.

Be sure to use a high quality rosin core solder (DO NOT use acid core solder), and a fine tipped low wattage (25 W or less) soldering iron.

The printed legend on the component side shows the exact position and orientation of each component. Check off each instruction step when completed.

() Solder in position the 1/4-watt 5% carbon film resistors:

| | | |
|-----|-----|-----------------------|
| R1 | 1K | (brown-black-red) |
| R2 | 1K | (brown-black-red) |
| R3 | 180 | (brown-grey-brown) |
| R4 | 180 | (brown-grey-brown) |
| R5 | 270 | (red-violet-brown) |
| R6 | 270 | (red-violet-brown) |
| R7 | 10K | (brown-black-orange) |
| R8 | 390 | (orange-white-brown) |
| R9 | 330 | (orange-orange-brown) |
| R10 | 330 | (orange-orange-brown) |
| R11 | 1K | (brown-black-red) |
| R12 | 100 | (brown-black-brown) |
| R13 | 180 | (brown-grey-brown) |

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| | | |
|-----|-----|-----------------------|
| R14 | 100 | (brown-black-brown) |
| R15 | 330 | (orange-orange-brown) |
| R16 | 330 | (orange-orange-brown) |
| R17 | 560 | (green-blue-brown) |

() Install forty-four IC sockets for IC3-IC43, RN1, RN2 and J1.

() Install the twenty-six capacitors. WHEN INSTALLING THE 10 mfd TANTALUM CAPACITORS MAKE CERTAIN THAT THE "+" END OF THE CAPACITOR IS ALIGNED WITH THE "+" PRINTED ON THE BOARD.

() Install SIP resistor networks RN3, RN4 and RN5. The arrow tips printed on the circuit board point to pin 1; align arrows with numerals "1" printed on the RN packages.

() Install Q1, a 2N3904 transistor, with the flat side facing the top of the board.

() Install the heatsink and voltage regulator ICs (IC1 and IC2) in the upper left-hand corner of the board. Make sure the regulator legs do not make contact with the metallic heat sink.

() Install the speed-select toggle switch just to the right of the heatsink.

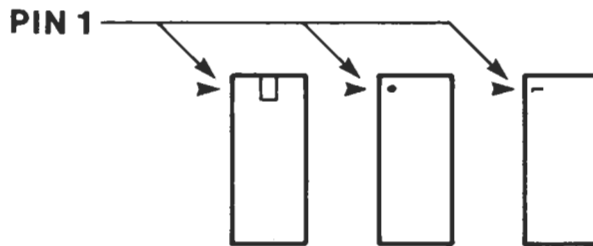
() Solder in position the 8.000 MHz crystal just to the

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right of the speed-select switch. Mechanically secure the crystal by soldering a short piece of number 24 wire to the hole on one side of the crystal, pull the wire tightly over the top of the crystal through the hole on the opposite side, then solder it in place.

() Install the four position Jump Address switch on the right side of the board. The arrow on the switch package indicating the ON position should point to the right.

() Install all ICs and resistor networks in their sockets (see Note below). The arrow tips printed on the circuit board point to pin 1 (see figure below).



After inserting the ICs and RNS, verify that they are all oriented in the same direction (pin 1 UP) with the exception of IC5 (pin 1 to the LEFT).

IMPORTANT NOTE

The most common assembly faults are bent-under IC and RN legs. To avoid this annoying problem, first bend the IC legs to closely match the IC socket span. Then "rock" the IC into its socket with a gentle end-to-end pressure. Visually inspect the legs after insertion by looking beneath the device.

This completes the construction of the Cromemco Z-80 CPU board. Carefully inspect your work before proceeding. Take particular care to see that there are no inadvertent solder bridges between pads and adjacent foil areas.

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ZPU PARTS LIST (REV E)

Capacitors

Part No.

| | | |
|---------|---------|----------|
| C1 | 10 uF | 004-0032 |
| C2 | .001 uF | 004-0022 |
| C3 | .005 uF | 004-0025 |
| C4 | .005 uF | 004-0025 |
| C5 | 0.1 uF | 004-0030 |
| C6 | 10 uF | 004-0032 |
| C7 | 150 pF | 004-0011 |
| C8 | 56 pF | 004-0006 |
| C9 | 10 uF | 004-0032 |
| C10 | 10 uF | 004-0032 |
| C11-C24 | 0.1 uF | 004-0030 |
| C25 | 150 pF | 004-0011 |
| C26 | 10 uF | 004-0032 |

Integrated Circuits

| | | |
|------|----------|----------|
| IC1 | LM340T-5 | 012-0001 |
| IC2 | LM340T-5 | 012-0001 |
| IC3 | 74164 | 010-0007 |
| IC4 | 74157 | 010-0009 |
| IC5 | Z-80A | 011-0010 |
| IC6 | 74LS04 | 010-0066 |
| IC7 | 74LS10 | 010-0063 |
| IC8 | 7400 | 010-0000 |
| IC9 | 7474 | 010-0019 |
| IC10 | 7404 | 010-0030 |
| IC11 | 74367 | 010-0080 |
| IC12 | 74367 | 010-0080 |
| IC13 | 74367 | 010-0080 |
| IC14 | 74367 | 010-0080 |
| IC15 | 74LS04 | 010-0066 |
| IC16 | 74157 | 010-0009 |
| IC17 | 74LS10 | 010-0063 |
| IC18 | 7400 | 010-0000 |
| IC19 | 7474 | 010-0019 |
| IC20 | 74LS04 | 010-0066 |
| IC21 | 7474 | 010-0019 |
| IC22 | 7408 | 010-0027 |
| IC23 | 74367 | 010-0080 |
| IC24 | 74367 | 010-0080 |
| IC25 | 74367 | 010-0080 |
| IC26 | 74367 | 010-0080 |
| IC27 | 74367 | 010-0080 |
| IC28 | 74S133 | 010-0089 |
| IC29 | 74164 | 010-0007 |
| IC30 | 7474 | 010-0019 |
| IC31 | 74LS04 | 010-0066 |

| | | |
|---------|--------|----------|
| IC32 | 7400 | 010-0000 |
| IC33 | 74LS04 | 010-0066 |
| IC34 | 74LS00 | 010-0069 |
| IC35 | 74LS02 | 010-0068 |
| IC36-41 | 74367 | 010-0080 |
| IC42 | 7408 | 010-0027 |
| IC43 | 74LS04 | 010-0066 |

Resistors

Part No.

| | | |
|-----|-----|----------|
| R1 | 1K | 001-0018 |
| R2 | 1K | 001-0018 |
| R3 | 180 | 001-0009 |
| R4 | 180 | 001-0009 |
| R5 | 270 | 001-0011 |
| R6 | 270 | 001-0011 |
| R7 | 10K | 001-0030 |
| R8 | 390 | 001-0013 |
| R9 | 330 | 001-0012 |
| R10 | 330 | 001-0012 |
| R11 | 1K | 001-0018 |
| R12 | 100 | 001-0007 |
| R13 | 180 | 001-0009 |
| R15 | 330 | 001-0012 |
| R15 | 330 | 001-0012 |
| R16 | 330 | 001-0012 |
| R17 | 180 | 001-0009 |
| R18 | 1K | 001-0018 |
| R19 | 180 | 001-0009 |

Resistor Networks

| | | |
|-----|----------|----------|
| RN1 | 4.7K DIP | 003-0017 |
| RN2 | 1K DIP | 003-0016 |
| RN3 | 1K SIP | 003-0007 |
| RN4 | 1K SIP | 003-0007 |
| RN5 | 330 SIP | 003-0004 |

ZPU INSTRUCTION MANUAL

Miscellaneous

| | |
|-----------------------|----------|
| Q1 2N3404 | 009-0001 |
| X1 8-MHZ XTAL | 026-0001 |
| SW1 SPDT SWITCH | 013-0000 |
| SW2 DIP SWITCH | 013-0001 |
| HEATSINK | 021-0017 |
| 6-32 SCREWS (4) | 015-0000 |
| 6-32 NUTS (4) | 015-0013 |
| #18 WIRE | 019-0012 |
| SOCKET 40 PIN | 017-0006 |
| 22-SOCKETS, 14 PIN | 017-0001 |
| 21-SOCKETS, 16 PIN | 017-0002 |
| ZPU PC BOARD | |

Software

CROMEMCO Z-80 MONITOR
(PAPER TAPE)

Documentation

Z-80 MONITOR MANUAL
ZPU INSTRUCTION MANUAL
Z-80A CPU TECHNICAL MANUAL

WARRANTY

Your factory-built ZPU is warranted against defects in materials and workmanship for a period of 90 days from the date of delivery. We will repair or replace products that prove to be defective during the warranty period provided they are returned to Cromemco. No other warranty is expressed or implied. We are not liable for consequential damages.

Should your factory-built ZPU fail after the warranty period, it will be repaired provided that it is returned to Cromemco, for a fixed service fee. We reserve the right to refuse to repair any product that in our opinion has been subject to abnormal electrical or mechanical abuse. The service fee is currently \$70.00 and is subject to change.

Your assembled ZPU kit will be repaired, provided that it is returned to Cromemco, for a fixed service fee. We reserve the right to refuse repair of any kit that in our opinion has not been assembled in a workmanlike manner or has been subject to abnormal electrical or mechanical abuse. Payment of the service fee must accompany the returned

ZPU INSTRUCTION MANUAL

merchandise. The service fee is currently \$70 and is subject to change.

ZPU™

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U.S. PATENT PENDING

SCHEMATIC REV. 4

BOARD REV. E

