

# Helios II

Model 2 (Part No. 300000)

Model 4 (Part No. 304000)

## Disk Memory System Manual

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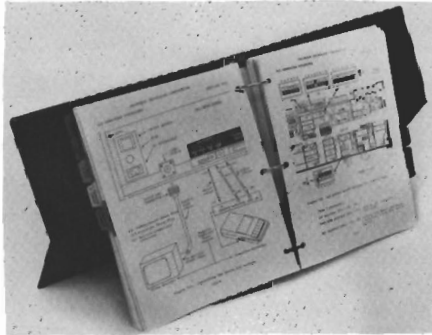
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## PREFACE

As a convenience feature for the user, this three-ring binder is an "easel" binder. The cover is hinged across the front and back as well as down the binding. You may find it helpful to stand up the binder in its easel position for two-handed operations when reference to the manual is necessary at the same time, as in the assembly sections, or troubleshooting.

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### IMPORTANT NOTE

The first part of this manual you should read is at the very end: the Updates section. Integrate this information into your manual before you begin.

The reader is invited to participate in the evolution of this manual. Please send your comments or suggestions for improvements to Processor Technology.

#### In Memoriam

This book is dedicated in grateful memory of Noel Leffler, a fine engineer and good person who is largely responsible for this book, but who died before his Helios II project was completed.

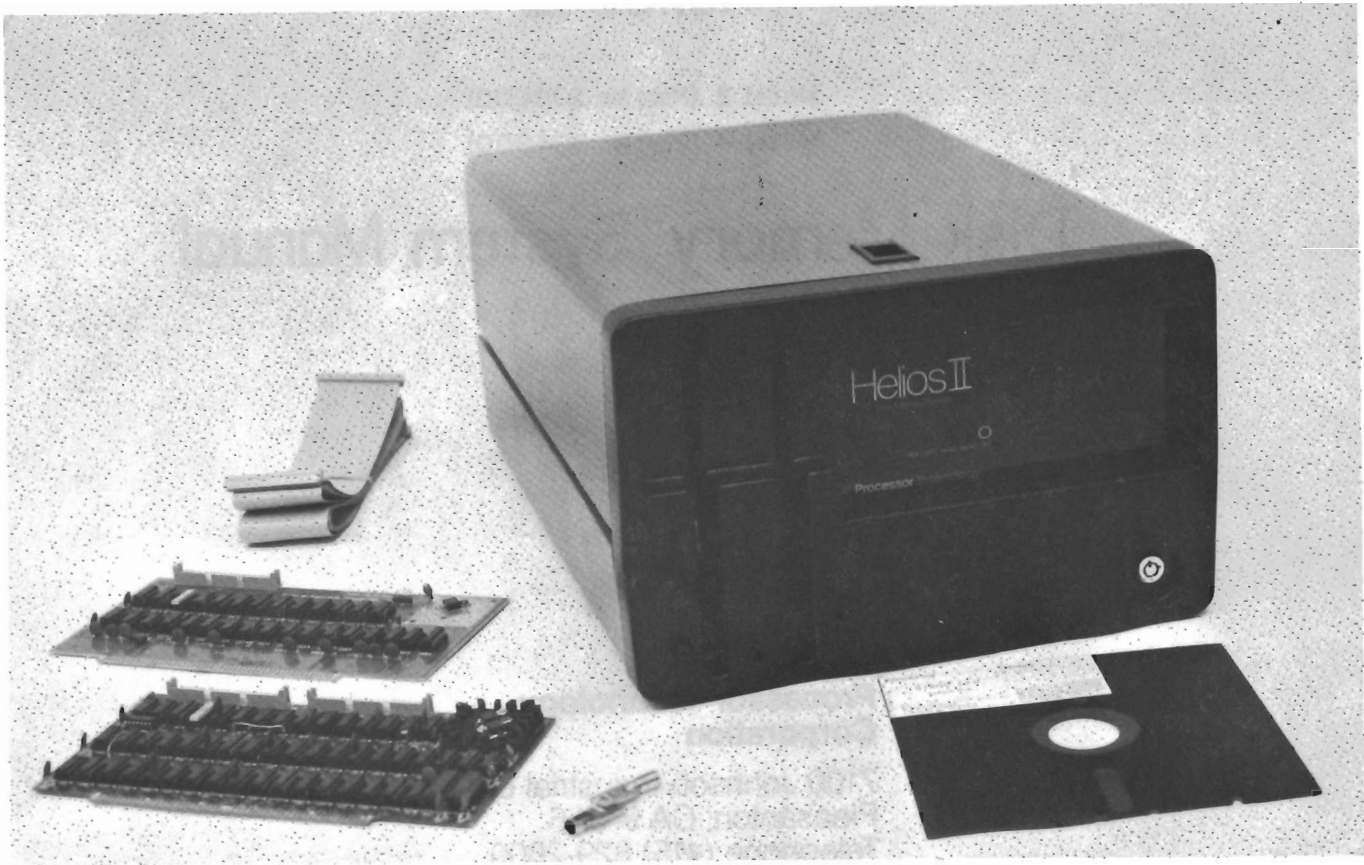


Fig. Ø Helios II System: Diskette Drive Cabinet, Controller and Formatter PCBs and Diskette containing PTDOS



## CONTENTS OUTLINE

Detailed contents precede each section.

### SECTION

- 1 INTRODUCTION
- 2 SPECIFICATIONS
- 3 ASSEMBLY AND TESTING
- 4 OPERATING INSTRUCTIONS
- 5 TESTING AND DIAGNOSTICS
- 6 MAINTENANCE
- 7 THEORY OF OPERATION
- 8 DRAWINGS
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- 10 UPDATES

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SOFTWARE MANUAL: PTDOS User's Guide

#### NOTE

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## ABBREVIATIONS

±	Plus or minus	CRC ERR	CRC Error
A	Ampere; Automatic; Address	CUTS	Computer Users Tape System
AC	Alternating current	CWE	Check Write Enable Signal on formatter, CRC gen.
ACI	Audio Cassette Interface		
ADDR DSBL	Address Disable	D	Display
A/R	As received	DC	Direct Current
Assy	Assembly	DI	Data Input
Aux	Auxiliary	DIO	Diode
AWG	American Wire Gage	DIP	Dual-In-Line Package
BC	Bit Counter	DMA	Direct Memory Access
BCTC	Bit Counter transmis- sion complete	DNSYNC	Name of a FF on the controller
Bin	Binary	DO	Data Output
BO	Bootload	DO DSBL	Data Out Disable
Br.	Bridge	DOS	Disk Operating System
BTU	British Thermal Unit	Drv	Drive
BUSTR	Bus Strobe	DS	Data Serial
C	Celsius (centigrade); Capacitor	EMI	electromagnetic interference
CC	Construction Counter	EO	Enable Output (Fifo signal)
CC DSBL	Command/Control Disable	EX-OR	exclusive OR
Cer	Ceramic	F	Fahrenheit
CF	Carbon film	Fab	Fabrication
CI	Command Interpreter	FF	Flipflop
Cm	Centimeter	FIFO	First-In, First-Out (LSI Buffer)
CNTR	Counter	FIFOPL	FIFO Parallel Load
Comm	Commoning	FIFO QS	Fifo Serial Output
Conn	Connector	Fig	Figure
CPSI	Clock Pulse Serial Input	ft	feet
CPSO	Clock Pulse Serial Output	FW	Flat Washer
CPU	Central Processing Unit	g	gravity (unit of measure)
CR	Carriage Return	GND	Ground
CRC	Cyclic Redundancy Check	Hex	hexidecimal
		HN	hex nut

HRR	Hold Request Resynchronized	NPN	Negative, Positive, Negative
Hz	Hertz (cycle)	ns	nanosecond
IC	Integrated Circuit	$\Omega$	ohm
ID	Identifier	OD	outside diameter
IESA	Input Enable Serial, A	OESA	Output Enable Serial, A (Fifo signal)
IESB	INPUT Enable Serial, B	OESB	Output Enable Serial, B (fifo signal)
Insul.	Insulated		
Inv	Inverter	ORE	Output Register Empty
I/O	Input/Output	P	Plug; Processor
IRF	Input Register Full	PC	Punctuation Counter
ITLW	Internal Tooth Lock Washer	PCB	Printed Circuit Board
J	Jack	PCHI	Signal on formatter
JK	Inputs to a JK Flipflop	PCL	Punctuation Counter L
K	kilobyte	PCQ	Punctuation Counter Output
Kg.	kilogram	PCX	Punctuation Counter X
kHz	kilohertz	PDBIN	Processor Data Bus In
LED	Light Emitting Diode	PHLDA	Processor Hold Acknowledge
LS	Low Power Schottky	PHLDAR	Delayed PHLDA
mA	milliamper	PHMS	Phillips Head Machine Screw
$\mu$ f	microfarad	PINTE	Processor Interrupt Enable (S-100 signal)
max.	maximum	PL	Parallel Load
MOS	Metal Oxide Semiconductor	Plex	plexiglas
MPX	multiplexer	POC	Power On Clear
MR	Master Reset (Fifo signal)	PRDY	Processor Ready
$\mu$ s	microsecond	PT	Processor Technology
ms	millisecond	PTDOS	Processor Technology Disk Operating System
MTBF	Mean Time Between Failures	PWAIT	Processor Wait (S-100 signal)
MTTR	Mean Time To Repair	PWR	Processor Write
N	number	Pwr	power
NA	Not Applicable; National Semiconductor		
NET	network		
No.	number		

Q	transistor; Output of a JK flipflop	TOS	Transfer Out Serial (Fifo Signal)
R	Resistor	TP	Test Point
RAM	Random Access Memory	TR	transfer
RCLOCK	Read Clock	TRANS COMM	transfer command
RDATA	Read Data	TTS	Transfer to Stock, FIFO signal
Recpt.	receptacle	U	Integrated Circuit
Rect.	Rectifier	UFO	Unidentified Flying Object
Reg.	regulator	UUT	Unit Under Test
REV	revision	φ2	Phase 2 (Signal on Controller)
RH	Relative Humidity	V	Volt(s)
RMC	Read missing clock	VAC	Volts AC
RND	Round	VCC	+5 V (Fifo pin)
rpm	revolutions per minute	VDC	Volts DC
RSECT	Sector Reset	VDM	Video Display Module
RQST	Request	VOM	volt/ohm meter
R/W	Read or Write	XCVR	transceiver
S	Seek; Status	XEQ	Execute
S-100	name of Intel standard 100-pin bus interface	XRDY	External Ready
SREADY	Status Ready		
SS	solid strand		
sec.	second		
SHLTA	Status Halt Acknowledge		
SINP	Status Input		
SINTA	Status Interrupt Acknowledge		
Sldr	solder		
SML	Status Machine Cycle 1		
SMEMR	Status Memory Read (S-100 signal)		
SOUT	Status Output		
SWO	Status Write Out (S-100) Signal		
SYNC	Synchronization		
Tant	tantalum		
TC	Transmission Complete		
TCSI	Transmission Complete Serial Input		
TOP	Transfer Out Parallel (Fifo Signal)		