DC5 Floppy Disk Controller
Introduction

The DC5 Floppy Disk Controller is an all-new design for the Southwest Technical Products Corp. 6800 and 6809 computers. It plugs into the SS-30 I/O bus and fully emulates the SWTPC DC4 controller. It supports double-sided, double-density disk for both 5.25-inch and 3.5-inch floppy drives. The DC5 will boot and run all SWTPC Disk Operating Systems (that were designed for the DC1 to DC4 controllers).

This new design uses a WD2797 that is a super set of the WD1797 and WD1691 chips that were used on the DC4. The earlier SWTPC controllers (DC1, DC2 and DC3) used the Western Digital FD1771 FDC chip that only supported single-density disks. The board was designed so that FD1771 chips could be used with a few cuts and jumpers.

A Programmable Logic Device was used to reduce chip count and make the printed circuit board, PCB, layout easier. A Xilinx XC9572 CPLD was chosen because the development tools are free, the chip is low cost and it is easily programmed in circuit. The design only uses about half of the XC9572 resources so additional features can be added in the future.

Switches and Jumpers

SW1 Position	Name	OFF - Logic High	ON - Logic Low
1	4-16	16 Addresses per port	4 Addresses per port
2	2Reg	Default DC-4 emulation	Enable second control register at 8016-8017 (E016-E017)
3	3.5 Inch	Use standard ribbon cable	Use IBM PC twisted ribbon cable for 3.5 inch drives
4	Cal	Normal Operation, WD2797 at 8018-801B (E018-E01B)	Calibration Timer at 8018-801B (E018-E01B)
5	Not used		spare
6	Test	Normal operation of WD2797	Alignment mode for WD2797

Note: Switch position 2 and 3 are different than in version 1 of the DC5. Position 4 is new. .

Note: SWPTC 6809 FLEX 2.8:1 will not work in double density mode with SW1-2 in the ON position (2Reg). A register bit, not SSO, controls the DDEN signal.

The 00 / 09 jumper selects the FDC ready signal from the Motor On signal in the 00 positions or from the Index Pulse in the 09 position.

Version 2 CPLD

The updated XC9572 adds a calibration timer so that no external test equipment is needed to align the DC5. You can tell the version of the CPLD by enabling the 2Reg mode (SW1 position #2) and reading location 8016-8017 (E016-E017). You will read a 02. Version 2 was released in December of 2001

In version 1 switch position #2 enable second control register when OFF. Switch position 3 used the twisted ribbon cable when OFF. You could read the version at location 8016 (E016).

There is no hardware difference between version 1 and 2. The DC5 can be updated by just reprogramming the CPLD

Installation

( ) If you will be using the disk unit with a 6800 (not 6809) processor board or with 3.5 inch floppy drives, install the Jumper in the “00” position. All other installations should have the Jumper in the “09” position.

Most 3.5 inch drives have a "feature" that makes them not work with a SWTPC DC-3 or DC-4 in the "09" jumper setting for the Ready line. These drives require the Ready jumper to be in the "00" position. The Index Pulse (pin 8) is "Masked" by a Seek Complete signal. In other words the Index Pulse signal is off during a Seek. (So is the Read Data.) Some of the older models had a jumper to control this but current production drives have no jumpers.

Current production drives that mask the Index Pulse during Seek operations and these will not work the stock SWTPC drivers in the “09” position. They work fine in the “00” position but you give up the disk missing from drive detection.

( ) If the motherboard has 4 address per slot (MP-B or MP-B2) SW1 position 1 should “ON”, for 16 address per slot is should be “OFF”

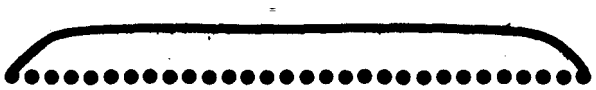
( ) If you are using standard SWTPC software SW1 position 2 should be “OFF”.

( ) If you are using an IBM style twisted ribbon cable SW1 position 3 should be “ON”

( ) All other SW1 positions should be “OFF”

( ) Unless specifically noted with a particular piece of software, the IRQ and FIRQ Jumper should be removed completely. Interrupts are presently not used with this board.

( ) In order for the DC5 to work properly with an SWTPC 6800 or 6809 computer with an MP-B or MP-B2 (not MP-B3 or MP-MB) motherboard, one minor modification needs to be made to the motherboard. With a short length of wire connect together each of the two end-pins of 30-pin I/0 connector row #5. This will connect the #5 port select line to UD3. When connecting the wire, route it around the PC support on the bottom of the board to prevent it from being pinched. Re-install the motherboard when finished. This modification should be done only on MP-B or MP-B2 motherboards.



( ) The disk controller board should now be plugged on to I/0 slot 6 on computers with MP-B or MP-B2 motherboards (4 addresses per slot) or I/0 slot 1 on computers with MP-MB or MP-B3 motherboards (16 address per slot).

( ) Connect the ribbon cable to the connector on the controller board. Route the cable through a hole in the rear of the computer or as desired. If the connector supplied on the cable does not have an indexing pin, install the connector so that pin 1 side should be nearer the front edge of the board when installed in the computer. When the controller board utilizes a connector that faces the rear of the computer, connect the cable such that the pin 1 side of the cable (banded side) goes toward the 1 marked on the rear mounting panel (toward the top of the computer).

With MP-B and MP-B2 motherboards the disk unit uses the ENABLE line from I/0 position 5 as a control line. Care should be exercised when using I/0 slot 5 for other devices.

IMPORTANT: Do not power the computer or disk units on or off while diskette are installed in the drives with the doors closed. Doing so may destroy any or all the data stored on the diskette(s).

6800 Boot Procedure

If you have the SWTBUG monitor ROM the boot command is a “D”. The built in boot is problematic and often fails. It attempts to load the first sector (track 0 sector 0) into RAM at $2400 then jumps to address $2400. Sometimes when it fails to load the sector it still jumps to $2400 and strange things happen. The biggest problem is that it does not allow enough time for the drive to come up to speed. The best workaround is to press “D”, wait a few seconds and see if boots. (You can hear the drive step from track to track.) If this fails press the RESET button try again. You may have to do this many times. (It is best to use a write protected boot disk.)

The bootstrap loader below seems to work every time.

```
* A BETTER 6800 BOOT LOADER
 8014            DRVREG  EQU    $8014     DRIVE REGISTER
 8018            COMREG  EQU    $8018     COMMAND REG 1771
 8019            TRKREG  EQU    $8019     TRACK REG 1771
 801A            SECREG  EQU    $801A     SECTOR REG 1771
 801B            DATREG  EQU    $801B     DATA REG 1771

 0300                    ORG    $0300
 0300 B6 80 18   START   LDA A  COMREG    TURN MOTOR ON
 0303 86 00              LDA A  #0
 0305 B7 80 14           STA A  DRVREG
 0308 CE 00 00           LDX    #$0000
 030B 08         OVR     INX
 030C 09                 DEX
 030D 09                 DEX
 030E 26 FB              BNE    OVR
 0310 C6 0F              LDA B  #$0F      RESTORE
 0312 F7 80 18           STA B  COMREG
 0315 8D 2C              BSR    RETURN
 0317 F6 80 18   LOOP1   LDA B  COMREG
 031A C5 01              BIT B  #1
 031C 26 F9              BNE    LOOP1
 031E 86 00              LDA A  #00
 0320 B7 80 1A           STA A  SECREG
 0323 8D 1E              BSR    RETURN
 0325 C6 9C              LDA B  #$9C      READ WITH LOAD
 0327 F7 80 18           STA B  COMREG
 032A 8D 17              BSR    RETURN
 032C CE 24 00           LDX    #$2400
 032F C5 02      LOOP2   BIT B  #2        DRQ?
 0331 27 06              BEQ    LOOP3
 0333 B6 80 1B           LDA A  DATREG
 0336 A7 00              STA A  0,X
 0338 08                 INX
 0339 F6 80 18   LOOP3   LDA B  COMREG
 033C C5 01              BIT B  #1        BUSY?
 033E 26 EF              BNE    LOOP2
 0340 7E 24 00           JMP    $2400
 0343 8D 00      RETURN  BSR    RTN
 0345 39         RTN     RTS
                         END    START
```

6809 Boot Procedure

The SBUG-E 6809 ROM monitor boot command is a “U”; the “D” is for the 8” inch DMA controller. FLEX for the 6809 boots from track 0 sector 1.

```
***** "U" MINIDISK BOOT *****
FBB3 7D   E018     MINBOOT TST    Comreg
FBB6 7F   E014             CLR    Drvreg    SELECT DRIVE 0

* DELAY BEFORE ISSUING RESTORE COMMAND
FBB9 C6   03               LDB    #3
FBBB 8E   0000             LDX    #0
FBBE 30   01       LOOP    LEAX   1,X
FBC0 8C   0000             CMPX   #0
FBC3 26   F9               BNE    LOOP
FBC5 5A                    DECB
FBC6 26   F6               BNE    LOOP

FBC8 86   0F               LDA    #$0F      *LOAD HEAD, VERIFY, 20msec/step
FBCA B7   E018             STA    Comreg    ISSUE RESTORE COMMAND
FBCD 8D   37               BSR    DELAY
FBCF F6   E018     LOOP1   LDB    Comreg    $FBCC
FBD2 C5   01               BITB   #1
FBD4 26   F9               BNE    LOOP1     LOOP UNTIL THRU
FBD6 86   01               LDA    #1
FBD8 B7   E01A             STA    Secreg    SET SECTOR REGISTER TO ONE
FBDB 8D   29               BSR    DELAY
FBDD 86   8C               LDA    #$8C      LOAD HEAD, DELAY 10msec,
FBDF B7   E018             STA    Comreg    AND READ SINGLE RECORD
FBE2 8D   22               BSR    DELAY
FBE4 8E   C000             LDX    #$C000
FBE7 20   09               BRA    LOOP3

FBE9 C5   02       LOOP2   BITB   #2        DRQ?
FBEB 27   05               BEQ    LOOP3
FBED B6   E01B             LDA    Datreg
FBF0 A7   80               STA    ,X+

FBF2 F6   E018     LOOP3   LDB    Comreg    FETCH STATUS
FBF5 C5   01               BITB   #1        BUSY?
FBF7 26   F0               BNE    LOOP2
FBF9 C5   2C               BITB   #$2C      CRC ERROR OR LOST DATA?
FBFB 27   01               BEQ    LOOP4
FBFD 39                    RTS
FBFE 8E   C000     LOOP4   LDX    #$C000
FC01 AF   4A               STX    10,U
FC03 1F   34               TFR    U,S
FC05 3B                    RTI

* DELAY
FC06 C6   20       DELAY   LDB    #$20
FC08 5A            LOOP5   DECB
FC09 26   FD               BNE    LOOP5
FC0B 39                    RTS
```

Users Manuals

The FLEX User's Guides can be found on the documentation page of the FLEX User's Group. http://www.flexusergroup.com) The hardware documentation can be found at http://www.swtpc.com.

6800 Memory Requirements

The memory requirements depend on which operating system you want to use. Good working memory is an absolute requirement. Run all the memory diagnostics that are in the SWTBUG User's Manual.

The original SWTPC FDOS requires 16k of ram from $0000 to $3FFF. If you are using an MP-S serial interface at port #1 you may have to patch a few programs. Look in the MP-A2 CPU board Assembly Instructions for details (pages 14 and 15).

MF-6800 FLEX 1.0 (MiniFLEX) requires 12k of RAM from $0000 to $2FFF and 4k of RAM from $7000 to $7FFF. It will work with an MP-C or MP-S interface at port #1.

TSC FLEX 2.0 requires 8k of RAM at $A000 to $BFFF and at least 12K of memory starting at $0000. The RAM on the CPU board will need to be disabled. The instructions are in the MP-A or MP-A2 documentation.

6809 Memory Requirements

TSC FLEX 9.0 requires 8k of RAM at $C000 to $DFFF and at least 12K of memory starting at $0000.

Floppy Disk Controller Alignment
(Using Internal Timer)

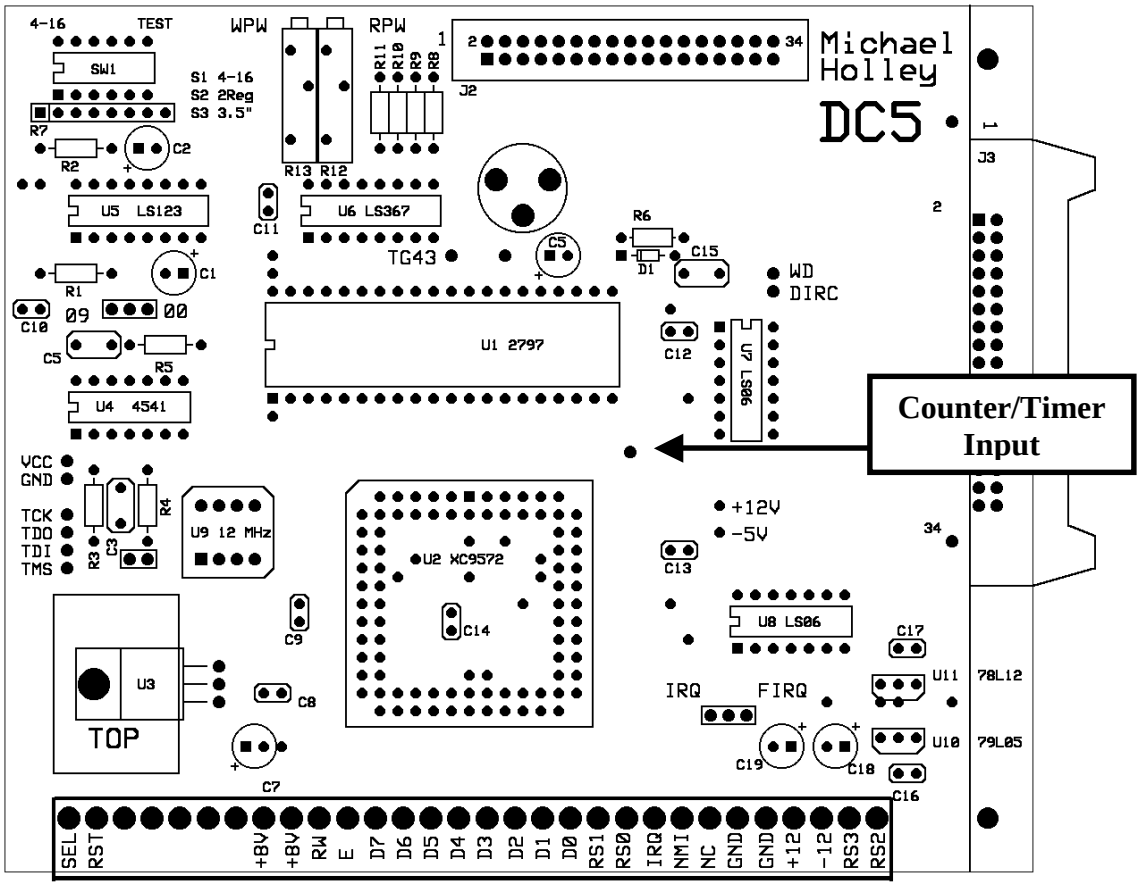
The XC9572 (U2) has a counter/timer that can be used to adjust the Write Precompensation and Data Separator. When the DIPswitch position 4 is "ON", the Counter/Timer is read at locations 8018-801B (E018-E01B) instead of the WD2797. The count is updated when a write is made to this location. This can be done manually but the short program below will display the value on the screen and make adjustment easier.

The counter/timer uses the 12 MHz clock and each unit is 83.3 ns. A count of 48 (30 hexadecimal) is 4000 ns or 4 µs. The input to the counter timer is the test point to the upper right of the XC9572 (U2).

Enter the desired program into memory. With the 6800 SWTBUG monitor you start a program with the J command (Enter J 0300). With the 6809 SBUG monitor you set the program counter to 0300 with a control P command then start with the G command.

If the value is always 00, perhaps the CAL switch (position #4) is "OFF". If the value is not responding to changes, perhaps the TEST switch (Position #6) is "OFF" or the RESET was pressed with the TEST switch ON. The 2Reg switch (Position #2) must be on to control the DDEN and 5/8 inputs to the 2797 chip.

To maintain internal VCO operation, insure that TEST is high (S1 position #6 OFF) whenever the RESET button is pushed.



```
                        NAM    DC5_CAL
                * MIKBUG / SWTBUG Routines for 6800
E0CA            OUT2HS  EQU    $E0CA
E19D            MCL     EQU    $E19D
E07E            PDATA1  EQU    $E07E
                * DC5 Counter Register
8018            FDC     EQU    $801A

0300                    ORG    $0300
0300 7F 80 1A   START   CLR    FDC       Start New Count
0303 CE FF FF           LDX    #$FFFF    Delay time
0306 09         LOOP    DEX              Wait for Count
0307 26 FD              BNE    LOOP
0309 B6 80 1A           LDA A  FDC       Get Value
030C B7 03 1D           STA A  STORE
030F CE 03 1D           LDX    #STORE
0312 BD E0 CA           JSR    OUT2HS    Print Value in Hex
0315 CE E1 9D           LDX    #MCL
0318 BD E0 7E           JSR    PDATA1    Print CR/LF
031B 20 E3              BRA    START
031D 00         STORE   FCB    0         Storage for Count
                        END    START
```

```
                      * SBUG-E Routines for 6809
               F80A   OUTCH   EQU    $F80A
               F80E   PCRLF   EQU    $F80E
                      * DC5 Counter Register
               E01A   FDC     EQU    $E01A

 0300                         ORG    $0300
 0300 7F   E01A      START   CLR    FDC       Start New Count
 0303 8E   FFFF              LDX    #$FFFF    Delay time
 0306 30   1F        DELAY   DEX              Wait for Count
 0308 26   FC                BNE    DELAY
 030A B6   E01A              LDAA   FDC       Get Value
 030D BD   0316              JSR    OUTHEX    Print HEX byte
 0310 AD   9F F80E           JSR    [PCRLF]   Print CR/LF
 0314 20   EA                BRA    START

                      * Print Acc A as HEX
 0316 B7   0331      OUTHEX  STAA   STORE     Save
 0319 44                     LSRA             Get upper HEX nibble
 031A 44                     LSRA
 031B 44                     LSRA
 031C 44                     LSRA
 031D 8D   05                BSR    XASCII
 031F B6   0331              LDAA   STORE
 0322 84   0F                ANDA   #$0F      Mask lower HEX nibble
 0324 8B   30        XASCII  ADDA   #$30      ASCII Addjust
 0326 81   39                CMPA   #$39      Is it < OR = "9"
 0328 2F   02                BLE    OUTC      If less, putput it
 032A 8B   07                ADDA   #7        If > Make ASCII letter
 032C AD   9F F80A   OUTC    JSR    [OUTCH]
 0330 39                     RTS
 0331 00             STORE   FCB    0
                             END    START
```

Floppy Disk Controller Alignment Using Internal Timer (Continued)

Write Precompensation

1. Set the TEST pin on to logic high by placing S1 (the DIP Switch) position #6 to OFF. (This is its normal position.) Also place S1 position #4 (Cal) to ON.
2. Press the computer reset button to strobe the MR pin.
3. Connect a jumper from the counter/timer input (upper right of U2) to the WD test pin.
4. Start the program by using SWTBUG / SBUG to jump to location $0300. The program will read the counter/timer about once a second and display a new hexadecimal value on your terminal.
5. Set the TEST pin to logic low by placing S1 position #6 to ON.
6. Adjust the WPW potentiometer to for the desired pulse width. (200ns) The WPW potentiometer is closest to the switch. Clockwise rotation decreases the pulse width. Adjust the potentiometer until the value changes from 3 to 2. This should be about 3 * 83.3ns or 250ns.
7. If you are going to adjust the Data Separator you can skip to step 5 below.
8. Set the TEST pin on to logic high by placing S1 position #6 to OFF. Also place S1 position #4 (Cal) to OFF.

Data Separator

1. Set the TEST pin on to logic high by placing S1 (the DIP Switch) position #6 to OFF. (This is its normal position.) Also place S1 position #4 to ON.
2. Connect a jumper for the counter/timer input (upper right of U2) to the TG43 test pin.
3. Press the computer RESET button to strobe the MR pin.
4. Set the TEST pin to logic low by placing S1 position #6 to ON.
5. Connect a jumper from the counter/timer input (upper right of U2) to the TG43 test pin.
6. Start the program by using SWTBUG / SBUG to jump to location $0300. The program will read the counter/timer about once a second and display a new hexadecimal value on your terminal.
7. Adjust the RPW potentiometer to for 1/8 of the read clock (1 µs for 5 ¼" SD.) The RPW potentiometer is closest to the 34–pin connector. Clockwise rotation decreases the pulse width. Adjust the potentiometer until the hexadecimal value changes from 0B to 0C. This should be about 12 * 83.3ns or 1000ns (1 µs)
8. Connect a jumper from the counter/timer input (upper right of U2) to the DIRC test pin.
9. Adjust the variable capacitor for Data Rate (125 kHz for 5 ¼" SD. A period of 8 µs. The waveform is high for 4 µs). Adjust the capacitor until the hexadecimal value reads 30. This should be 48 * 83.3ns or 4000ns (4 µs).
10. Set the TEST pin on to logic high by placing S1 position #6 to OFF. Also place S1 position #4 to OFF.

NOTE: To maintain internal VCO operation, insure that TEST is high (S1 position #6 OFF) whenever the RESET button is pushed

NOTE: The values on TG43 and DIRC depend on the states of the DDEN and 5/8 pins. They should both be low after reset. You can control the pins by enabling the second control register (place S1 position #2 to ON) and writing the values given in the table on page 11 to address 8017 or E017.

Floppy Disk Controller Alignment
(Using an Oscilloscope)

Write Precompensation

1. Set the TEST pin on to logic high by placing S1 (the DIP Switch) position #6 to OFF. (This is its normal position.) Also place S1 position #2 to ON.
2. Press the computer reset button to strobe the MR pin.
3. Set the TEST pin to logic low by placing S1 position #6 to ON.
4. Observe the pulse width on the WD test pin.
5. Adjust the WPW potentiometer to for the desired pulse width. (200ns) The WPW potentiometer is closest to the switch.
6. Set the TEST pin on to logic high by placing S1 position #6 to OFF.

Data Separator

1. Set the TEST pin on to logic high by placing S1 (the DIP Switch) position #6 to OFF. (This is its normal position.) Also place S1 position #2 to ON.
2. Press the computer RESET button to strobe the MR pin.
3. Set the TEST pin to logic low by placing S1 position #6 to ON.
4. Observe the pulse width on the TG43 test pin.
5. Adjust the RPW potentiometer to for 1/8 of the read clock (1us for 5 ¼" SD.) The RPW potentiometer is closest to the 34–pin connector.
6. Observe the frequency on the DIRC.
7. Adjust the variable capacitor for Data Rate (125 kHz for 5 ¼" SD. A period of 8 microseconds)
8. Set the TEST pin on to logic high by placing S1 position #6 to OFF.

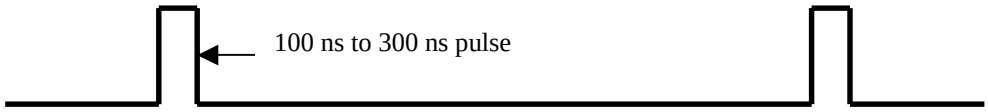
NOTE: To maintain internal VCO operation, insure that TEST is high (S1 position #6 OFF) whenever the RESET button is pushed

NOTE: The values on TG43 and DIRC depend on the states of the DDEN and 5/8 pins. They should both be low after reset. You can control the pins by enabling the second control register (place S1 position #2 to ON) and writing the values given in the table on page 11 to address 8017 or E017.

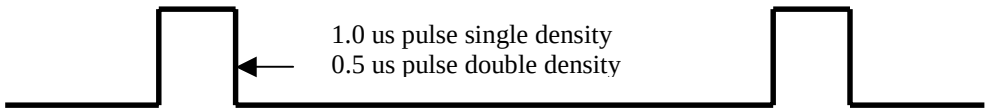
NOTE: Proper operation requires these adjustments. If you do not have the test equipment to measure pulse width and frequency you can try the following. Adjust the WPW potentiometer to set the voltage level at WD2797 pin 33 to 2.5 volts. Adjust the RPW potentiometer to set the voltage level at WD2797 pin 18 to 2.5 volts. Rotate the variable capacitor so the soldered part of the rotor is at 2 o'clock.

The values for alignment may be changed setting by the levels on the DDEN and 5/8 pins. After a reset, 5/8 and DDEN are low. Set S1 position 2 “ON”, enabling the second control register. Using the ROM monitor (SWTBUG or SBUG-E) to write the hex word below to address 8017 or E017. (A write to this location will not verify, you will read the INTRQ and DRQ status.)

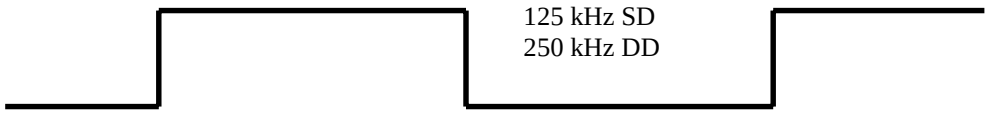
DDEN	5/8	Hex word	DIRC frequency	DIRC period	TG43 pulse width
0	0	00	125 kHz	8 us	1.0 us
0	1	10	250 kHz	4 us	0.5 us
1	0	20	250 kHz	4 us	0.5 us
1	1	30	500 kHz	2 us	0.25 us



Waveform on WD test point



Waveform on TG43 test point



Waveform on DIRC test point

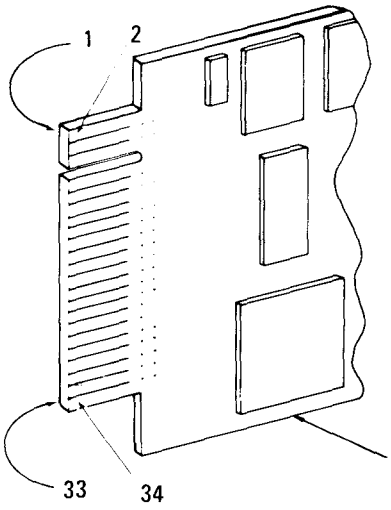
Replacing the WD2797 with a FD1771

Pin	WD2797	FD1771	Description
1	Enable Precomp (ENP)	VB -5 Volts	Cut the trace between pin 1 and pin 29 on the bottom of the board near pin 1. Add a wire jumper to the –5 volt supply.
17	5/8 Select (5/8)	Phase 3 (PH3)	The CPLD pin connected to this pin should be tri-state.
18	Read Pulse Width (RPW)	3-Phase Motor Select (3PM#)	This pin should be at a logic level high or open. Adjust the RPW pot to above 3 volts.
23	Pump	Head Load Timing (HLT)	Remove C5, connect a jumper wire from pin 23 to the top via above pin 40. The lower via should be 12 volts. Make sure the trace between the two vias is cut.
25	Side Select Output (SSO)	External Data Separation (XTDS#)	The CPLD pin connected to this pin should be high or tri-state.
26	Voltage Controlled Oscillator (VCO)	Floppy Disk Clock (FDCLOCK)	Connect to +5 volts
33	Write Precomp Width (WPW)	Write Fault (WF#)	This pin should be at a logic level high. Adjust the WPW pot to above 3 volts.
37	Double Density (DDEN#)	Disk Initialization (DINT#)	The CPLD pin connected to this pin should be high.
40	Head Load Timing (HLT)	VDD +12 Volts	Cut the trace between pin 40 and the U5 (74LS123) on the bottom of the board above pin 40. Leave one via connected to pin 40. Add a wire jumper between the via above pin 40 and the 12 volt supply. The other via is used for HLT.

Active low signals have a trailing '#'.

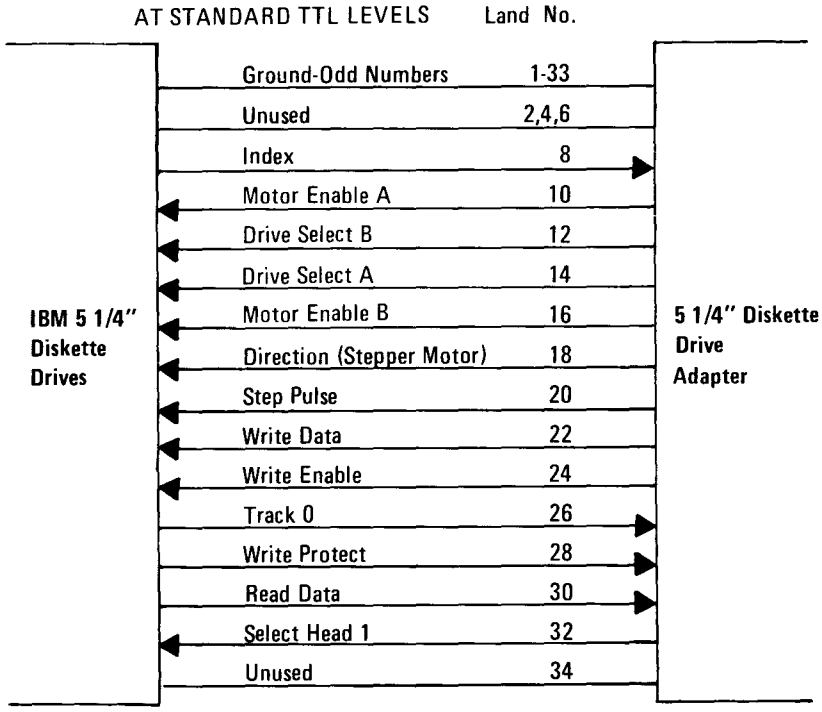
This procedure has not been tested.

5-1/4" Diskette Drive Adapter
Internal Interface Specifications



34 PIN KEYED
EDGE CONNECTOR

NOTE: LANDS 1–33 ARE ON THE BACKSIDE OF THE BOARD, LANDS 2–34 ARE ON THE FRONT, OR COMPONENT SIDE.



2-112

Figure from IBM PC Technical Reference - 6025008 (July 1982)

From page 2-110. All adapter outputs are open-collector gates (7438). Each adapter input is terminated with a 150-ohm resistor to VCC.