EG&G RETICON

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OPERATION AND MAINTENANCE MANUAL MC520/RS520 CAMERA/CONTROLLER SYSTEM

SAFETY CONSIDERATIONS

CAUTION

BEFORE SWITCHING ON THIS INSTRUMENT:

1. MAKE SURE THE INSTRUMENT IS SET TO THE VOLTAGE OF THE POWER SOURCE

2. ENSURE THAT ALL DEVICES CONNECTED TO THIS INSTRUMENT ARE CONNECTED TO THE PROTECTIVE (EARTH) GROUND.

3. THE PROTECTIVE EARTH TERMINALS OF THE INSTRUMENT MUST BE CONNECTED TO THE PROTECTIVE CONDUCTOR OF THE (MAINS) POWER CORD. THE MAINS PLUG SHALL ONLY BE INSERTED IN A SOCKET OUTLET PROVIDED WITH A PROTECTIVE EARTH CONTACT. THE PROTECTIVE ACTION MUST NOT BE NEGATED BY THE USE OF AN EXTENSION CORD (POWER CABLE) WITHOUT A PROTECTIVE CONDUCTOR (GROUNDING).

4. MAKE SURE THAT ONLY FUSES WITH THE REQUIRED RATED CURRENT AND OF THE SPECIFIED TYPE (NORMAL BLOW, TIME DELAY, ETC.) ARE USED FOR REPLACEMENT. THE USE OF REPAIRED FUSES AND THE SHORT-CIRCUITING OF FUSE HOLDER MUST BE AVOIDED.

WARNING

THE SERVICE INFORMATION FOUND IN THIS MANUAL IS OFTEN USED WITH POWER SUPPLIED AND PROTECTIVE COVERS REMOVED FROM THE INSTRUMENT. ENERGY AVAILABLE AT MANY POINTS MAY, IF CONTACTED, RESULT IN PERSONAL INJURY.

WARRANTY

Reticon warrants that the camera described herein will be free from defects in material and workmanship under normal use and service for a period of one year from date of shipment. The liability of Reticon under this warranty is limited solely to replacing or repairing or issuing credit (at the discretion of Reticon) for such parts that become defective during the warranty period. In order to permit Reticon to properly administer this warranty, Buyer shall: (1) Notify Reticon promptly in writing of any claims; (2) Provide Reticon with an opportunity to inspect and test the camera claimed to be defective. Such inspection may be on customer's premises or Reticon may request return of the camera at the customer's expense. Such expenses will subsequently be reimbursed to customer if the camera is found to be defective. Adjustment is contingent upon Reticon's examination of the product, disclosing that apparent defects have not been caused by misuse, abuse, improper installation or application, repair, alteration, accident or negligence in use, storage, transportation or handling. In no event shall Reticon be liable to Buyer for loss of profits, loss of use, or damages of any kind based upon a claim for breach of warranty.

THIS WARRANTY IS EXPRESSED IN LIEU OF ALL OTHER WARRANTIES EXPRESSED OR IMPLIED, INCLUDING THE IMPLIED WARRANTY OF FITNESS FOR A PARTICULAR PURPOSE, AND OF ALL OTHER OBLIGATIONS OR LIABILITIES ON RETICON'S PART, AND IT NEITHER ASSUMES NOR AUTHORIZES ANY OTHER PERSON TO ASSUME FOR RETICON ANY OTHER LIABILITIES IN CONNECTION WITH THE SALE OF THE SAID CAMERA.

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SECTION I

SYSTEM STARTUP

1.1 UNPACKING

Carefully remove the MC 520 Camera and RS 520 Controller from their shipping boxes and inspect them for any visual damage. Remove the two fasteners holding the controller top cover and inspect the interior for any damage. Assure that the two P/C boards in positions A4 and A6 are properly seated in their connectors.

Immediately report any shipping damage to the common carrier who delivered the equipment, and to Reticon, describing type and extent of damage. Reticon will then determine disposition and means of repair.

1.2 POWERING UP

If no damage is found, install the camera lens, and connect the camera to the controller with the interconnecting cable provided. The camera connector is clearly marked on the controller rear panel, and a similar connector is easily recognized on the camera rear panel. Also connect the X,Y,Z, BNC outputs of the controller to a video monitor.

Make sure the line voltage selector switch on the controller rear panel is set for the required voltage, and the correct fuse is installed for the selected voltage, 2 amp. for 115 VAC and 1 amp. for 220 VAC.

Connect the controller to the AC line with the cable provided and depress the red power switch on the controller front panel. Note that the red indicator lamp illuminates.

1.3 SYSTEM CHECKOUT

Perform a rough system checkout as follows: Set the lens to its smallest f/number, and point the lens at an intense light source such as a lamp, flashlight, or match flame. Note that the green light level indicator illuminates on the controller front panel.

Set the lens to its largest f/number and observe that a raster is on the monitor screen previously connected to the controller. Adjustment of the monitor contrast and focus controls may be necessary to see the raster clearly. Also, adjustment of the controller X and Y gain controls may be necessary to obtain a picture of proper size. These adjustments are clearly

marked on the card retainer plate at the edge of the controller A6 P/C board. Be sure not to adjust any other controls at this time.

"Look" at a well lighted scene with the camera, preferably an outdoor scene where sunlight assures enough illumination intensity. While observing the picture on the monitor, adjust the lens focus and f/number until a good picture is obtained. The data rate has been set at the factory to 1 MHz, which should give sufficient sensitivity for the outdoor scene on a sunny day. This frequency can be changed to any value between 0.25-5 MHz and these adjustments will be described in later sections of the manual. Observance of a good monitor picture concludes the rough system checkout.

SECTION II

INTRODUCTION

2.1 MC520/RS520 SYSTEM

The MC520 Camera and RS520 Controller form the MC520/RS520 system which has many applications in high resolution, high speed, non-contact measurement of size, shape, and position.

These applications include:

Automatic Semiconductor Bonding
Laser Beam Profiling
Optical Surface Inspection
Finger/Palm Print Recognition
Blood Cell/Bacteria Colony Counting
Security Observation
Ink Print Quality Determination
Robot Arm Vision.

Basically, any object or pattern may be inspected if it has contrast against its background.

2.2 MC520 CAMERA - GENERAL

The MC520 Camera, Figure 1, is about the size of and operates similar to an ordinary photographic camera, with the exception that the film is replaced by an array of 10,000 photodiodes arranged in a 100 x 100 pattern on 2.4 mil (60 μm) center-to-center spacing.

The accuracy of measurement is determined by the field of view, which can range from a fraction of an inch to many feet depending on the working distance. For example, with a 5 inch (127mm) field of view, size differences of 0.05 inch (1.27mm) can be resolved, and with a 0.5 inch (12.7mm) field of view, 0.005 inch (127μm) can be resolved.

The field of view is imaged through the lens onto the photodiode array which is electronically scanned by signals from the RS520 Controller at data rates adjustable from 0.25-5 MHz. (25-500 Frames/Second.)

2.2.1 MC520 Mechanical Configuration

The MC520 is enclosed in a cast aluminum, environmentally protected enclosure with dimensions shown in Figure 2.

Camera construction is ruggedized for industrial environments, and with optional lens cover it is sealed against intrusion of dust and moisture.

The camera is available in both "C" and "V" versions. The "C" version will accept both "C" and "U" mount lenses, and one "C" mount lens with the following choice of focal lengths is supplied with the camera: 8.5, 12.5, 25, 50, or 75mm.

The "V" version provides a through the lens viewer similar to that of a reflex type photographic camera, enabling the operator to see the subject directly through the camera lens. A reticle in the viewer outlines the area actually scanned by the 100 x 100 sensor array. The "V" camera accepts "U" mount lenses only.

Camera mounting is accomplished by means of four 6-32 screws, or a 1/4-20 threaded tripod mount, as shown in Figure 2.

2.2.2 MC520 Electronic Configuration

The MC520 electronics, Figure 3, are contained on three printed circuit cards mounted within the housing. These electronics process data from the 100 x 100 sensor on command from the RS520 controller.

The array is scanned at a rate determined by clock pulses from the controller and may be set to any value from 0.25 -5MHz. The camera video output is a train of sampled-and-held pulses with an amplitude proportional to light intensity and frame integration time. A long scan time is desirable for high sensitivity, while a short time is desirable to obtain a sharp image of a rapidly moving object. The frame scan time can be set to any value between 2 and 40 milliseconds.

The specific characteristics of the application, such as light level, and rate of object motion, will determine the optimum value. See Section V for a discussion of optical parameters.

Signals enter and exit the camera through an 18 pin Bendix connector, J4, located on the camera rear panel, and additionally three BNC connectors provide test points for setup and servicing the camera. These test points and their functions are shown in Figure 2. A more detailed discussion of camera electronics will be found in Section VII, Principles of Operation.

2.3 RS520 CONTROLLER - GENERAL

The RS520 Controller, Figure 4, provides electronics P/C boards, power supply, and data I/O connectors to operate the MC520 camera when it is connected to the camera I/O connector.

Three spare P/C board positions and additional power are available to the user for building his own system within the controller housing if desired. See Section IV for power specifications.

2.3.1 RS 520 Mechanical Configuration

The RS 520 Controller is enclosed in a bench top cabinet with dimensions shown in Figure 5. Optional standard 19 inch rack mounting hardware is also available if desired.

2.3.2 RS 520 Electronic Configuration

RS 520 electronics, Figure 6, are contained on two P/C boards in positions A4 and A6. Position A4 is the Digital Board which generates clock and synchronizing signals to the camera, and re-synchronizes with signals from the camera to control the video processing and sweep circuits on the Analog Board in position A6. An additional P/C board position, A5, is present for A/D option P & S.

An interconnect P/C board on the rear of the P/C board connector bracket contains ± 10 volt regulators for the A6 board, and also provides signal connection between the A4, 5, and 6 board connectors. The controller will operate the MC 520 camera at data rates from 0.25-5MHz, while providing video and synchronizing signals for transmission over up to 100 feet (30m) of additional cable between controller and users equipment. The controller also provides X,Y, and Z output signals for direct connection to a video monitor. A more detailed discussion of controller electronics will be found in Section VIII, Principles of Operation.

SECTION III

MC 520 CAMERA SPECIFICATIONS

3.1 MECHANICAL

Dimensions	3.58 x 3.8 x 3.75 inches (9.09 x 9.65 x 9.53 cm.)
Mounting	Four 6-32 screws on a 2.25 inch (57.15 mm) square, or a 1/4-20 threaded tripod mount.
Weight	1.5 lbs. (0.68Kg).

3.2 OPTICAL

Array Size	10,000 pixels arranged in a 100 x 100 matrix.
Spacing	2.4 mils (60 μm) center-to-center in X or Y direction.
Active Area	0.24 x 0.24 inches (6 x 6 mm.)
Saturation Exposure	0.25 μw-sec/cm^2 @ 2870K typical. See Figure 7 for transfer characteristic.
Blooming Characteristic	See Figure 8 and description of measurement in 5.2.2.

3.3 ELECTRICAL

3.3.1 BNC Connectors

3.3.1.1 Video

The Video BNC is connected to one side of the differential line driver output, hence its signal to noise ratio will not be as good as at the controller after the differential line receiver. As a result, the Video BNC output is intended as a test point only to assure that the camera is generating video properly to the controller.

Saturated Light Level	Adjustable to 2V p-p, AC coupled, 1K Ω load min.

Dark Level	0 volts ± 30 mv.
Scanning Rate	0.25-5 MHz, determined by clock frequency from controller.

3.3.1.2 Frame Sync

Level	+2.4 volts min. during line 100, +0.8 volts max. during lines 1-99. 1KΩ load min.
Pulse Period	100 line intervals.
Pulse Width	One line interval.

3.3.1.3 Line Sync

Level	+2.4 volts min. during line retrace, +0.8 volts max. after retrace. 1KΩ load min.
Pulse Rate	Line rate.
Pulse Width	Equal to width of M1C pulse from controller, adjustable from 3 to 15 pixel periods in controller.

3.3.2 Bendix Connector, J4

The Bendix connector, on the camera rear panel, carries power, video, and sync signals between the camera and controller. Cable length can be determined from the following formula:

$$\text{length in feet} = \left[\frac{227}{\text{FMHz}} - 16\right] \text{ or 75 feet, whichever is less.}$$

FMHz is the maximum data rate used. Recommended cable type is Belden 8774. An 8 foot length with connectors is supplied with the system. Other lengths are optionally available.

3.3.2.1 Analog Signals

The differential video output is designed to be received by the controller analog line receiver. The following video specifications are at the output of this receiver, which removes connecting cable induced noise. The output of the receiver is on the controller A6 P/C board, Test Point 1.

3.3.2.1.1 Video (+) and (-) Outputs (Exits camera on pins G & H respectively; specs are at TP-1 as described above)

Saturated Light Level	2 volts p-p, AC coupled, averaging around dark level.
Dark Level	+3 volts nominal
Dynamic Range	≥ 200:1
Ramdom Noise	≤ 10 mv p-p
Coherent Noise	≤ 200 mv p-p
Scanning Rate	0.25-5MHz
Settling Time	≤ 120 ns to 95% of saturation level.
DC Restoration	Provided by controller video processing.

3.3.2.2 Digital Signals

The camera digital I/O signals are transmitted or received by μA9638 or μA9637 line transmitters or receivers respectively. The camera provides 100 Ω terminations for signals received, and the R5520 Controller provides 100 Ω terminations for camera transmitted signals.

3.3.2.2.1 MCLK (+) and (-) Inputs (Pins M and N respectively)

Level	This is the X scan clock input to be driven by a μA9638 line transmitter or equivalent device meeting EIA-RS-422 specifications.
Pulse Rate	0.25-5MHz, set by controller master clock frequency control.
Pulse Width	100 ns minimum, set by controller master clock pulse width control.

3.3.2.2.2 M1C(+) and (-) Inputs (Pins P and U respectively)

Level	This is the Y scan clock input to be driven by a μA9638 line transmitter or equivalent device meeting EIA-RS-422 specifications.

Pulse Rate — Line scan rate, 25-500 per second depending on X scan rate set by controller.

Pulse Width — Set by controller retrace counter and adjustable 3-15 pixel intervals. Count is determined by:

Count minimum = 2 (FMHz +1), where FMHz is maximum X scan rate required. For 5 MHz, this count would be 2(5+1) = 12 minimum.

3.3.2.2.3 CCLK (+) and (-) Outputs (Pins B and C respectively)

Level — This is a re-transmission of the camera MCLK input which is used by the controller to re-synchronize the data and remove cable propagation delay differences. It is received by a μA9637 line receiver or equivalent device meeting EIA-RS-422 specifications.

Pulse Rate — Same as MCLK signal. (3.3.2.2.1)

Pulse Width — Same as MCLK signal. (3.3.2.2.1)

3.3.2.2.4 EOF (+) and (-) Outputs (Pins K and L respectively)

Level — This is the End of Frame sync signal output generated by the 100 x 100 array, and is used to synchronize the controller. It is received by a type μA9637 or equivalent line receiver meeting EIA-RS-422 specifications.

Pulse Rate — Frame Rate, 25-500 per second.

Pulse Width — One line interval (true during line 100).

3.3.2.3 Power

The camera requires nominally +5, +15, and -15 volts which is supplied by the controller when the camera is connected to it. Voltage tolerances, regulation, and current requirements are as follows:

3.3.2.3.1 +5 Volts and Digital Ground (Pins T and J respectively)

Voltage Setting	+5 volts ± 5%
Voltage Regulation	≥ 1%
Current	250 ma maximum

3.3.2.3.2 +15 Volts (Pin E)

Voltage Setting	+15 volts ± 5%
Voltage Regulation	≥ 1%
Current	150 ma maximum

3.3.2.3.3 -15 Volts and Analog Ground (Pins R and S respectively)

Voltage Setting	-15 volts ± 5%
Voltage Regulation	≥ 1%
Current	100 ma maximum

3.4 ENVIRONMENTAL

3.4.1 Temperature

Operating Ambient	0 to 50°C
Storage	-20 to +100°C

3.4.2 Humidity

90% R.H. Non-Condensing, Camera is splash resistant

3.5 ADJUSTMENTS

3.5.1 Internal

A1 Board	LR/LT (R14), Gain Balance (R33) ØY Balance (C34)
A2 Board	VQ (R20), VQ Balance (R19) VBB (R21), VBUF (R23) VIRIS Zero (R5)

External

A3 Board	Gain (R20)

SECTION IV

RS520 CONTROLLER SPECIFICATIONS

4.1 MECHANICAL

Dimensions	16.9 x 5.6 x 16.7 inches (42.93 x 14.22 x 42.42 cm.)
Mounting	Bench top, or with optional hardware can be mounted in standard 19 inch rack.
Weight	22.5 lbs. (10.2 kg)

4.2 ELECTRICAL

4.2.1 BNC Connectors

4.2.1.1 Z Output

The Z output is a series of sampled and held video pulses having amplitudes proportional to the light intensity on each pixel and the frame integration time. Specifications are with a 50 ohm termination.

Blank Level	Adjustable +0.1 volts to -1 volt, Drift $\leq$ 0.5mv/^{o}C.
Dark Level	Adjustable +0.1 volts to -1 volt, Drift $\leq$0.5mv/^{o}C.
Saturation Level	Adjustable to +1 volt above dark level.
Dynamic Range	$\geq$ 200:1
Random Noise	$\leq$ 5 mv p-p
Coherent Noise	$\leq$ 50 mv p-p
Data Rate	0.25 -5MHz
Settling Time	< 50 ns to 95% of saturation level.

The X,Y, and Z outputs may be directly connected to a monitor for presentation of the camera field of view.

4.2.1.2 Y Output

The Y output is a linear ramp synchronized with the camera frame rate, and is intended to provide Y axis sweep for a monitor presentation of the camera field of view. Specifications are with 50 ohm termination.

Retrace Level	0 volts $\pm$ 50 mv
Peak Ramp Level	Adjustable to $\pm$ 1 volt
Linearity	Within 2% of best straight line.

Ramp automatically maintains level with scan rate changes. Y output is not usable if camera external start mode is used and camera is stopped for longer than $\left[\frac{1}{\text{FMHz}}\right]$ milliseconds, where FMHz is data rate; i.e., at 5 MHz, maximum stop interval would be $\frac{1}{5}$ millisecond.

4.2.1.3 X Output

The X output is a linear ramp synchronized with the camera line rate, and is intended to provide X axis sweep for a monitor presentation of the camera field of view. Specifications are with 50 ohm termination.

Retrace Level	0 volts $\pm$ 50 mv
Peak Ramp Level	Adjustable to $\pm$ 1 volt
Linearity	Within 2% of best straight line.

Ramp automatically maintains level with scan rate changes. X output is not usable if camera external start mode is used and camera is stopped for more than $\left[\frac{1}{\text{FMHZ}}\right]$ milliseconds, where FMHz is data rate; i.e., at 0.5 MHz, maximum stop interval would be $\frac{1}{0.5}$ ms. = 2 milliseconds.

4.2.1.4 75 Ω Output

The 75 ohm output is a differential presentation of the Z output (4.2.1.1) and is intended for driving up to 100 feet of cable. Recommended cable is Belden 9272 or equivalent. Specifications are with 75 ohm termination and differential output. Shield should be connected to users chassis ground, and the analog ground in either the Data A or Data B connector to user signal ground.

Blank Level	Adjustable +0.2 to -2 volts, Drift $\leq$ 0.5mv/^{o}C.
Dark Level	Adjustable +0.2 to -2 volts, Drift $\leq$ 0.5mv/^{o}C.
Saturation Level	Adjustable to +2 volts above dark level.
Dynamic Range	$\geq$ 200:1

Random Noise	≤ 10 mv p-p
Coherent Noise	≤ 100 mv p-p
Data Rate	0.25 - 5 MHz
Settling Time	< 50 ns to 95% of saturation level.

If the 75 ohm output is used, the differential output on Data B connector cannot be used simultaneously.

4.2.1.5 Threshold

The threshold output is the DC level used by the Data level detector to determine the data threshold. This output is presented through a 10 KΩ resistor, and must not be loaded if accurate threshold measurements are to be obtained.

Level	Adjustable 0 to +2 volts

If the threshold level is compared to the unterminated Z output, a ± 30 mv error in threshold setting can occur. A more accurate measurement can be made by comparing the threshold level to the video at TP-5 on the A6 board.

4.2.1.6 Sync

The Sync output is the controller Frame Enable signal presented through a 50 ohm resistor from a TTL buffer. Specifications are with 1KΩ load.

Level	+2.4 volts minimum during Frame Enable, +0.8 maximum during line 100 retrace.
Pulse Rate	Frame Rate, 25-500 per second.
Pulse Width	100 line intervals

4.2.2 Bendix Connectors

4.2.2.1 Data A Connector

The Data A Connector I/O signals are plug to plug compatible with Reticon Automatic Measurement Systems. These signals of course can be

connected directly to the users equipment as well. See Figure 9 for a timing diagram showing their relationship to the camera video. All signals in this connector are digital and differential. Up to 100 feet of Belden 8774 cable may be used, and all shields should be connected to the connector shells only. See Figure 28.

4.2.2.1.1 Digital Ground (Pin A)

This is the common digital return for all signals in the Data A connector.

4.2.2.1.2 ECLK (+) and (-) Inputs (Pins E and F respectively)

Level	To be driven by a μA9638 line transmitter or equivalent device meeting EIA-RS-422 specifications. This signal will synchronize the camera with the users external clock. Switch selection of external clock (ECLK) must be made on Switch S1-C4 of the controller A4 P/C board. See Table I, "S1 switch settings."
Pulse Rate	0.25 -5 MHz
Pulse Width	≥ 100 ns

4.2.2.1.3 Data (+) and (-) Outputs (Pins H and G respectively)

Level	This is the Binary Data Output signal, logically true for pixels above threshold, logically false below threshold. To be received by a μA9637 or equivalent device meeting EIA-RS-422 specifications.
Pulse Period	Variable, depending on video levels.
Pulse Width	Variable, depending on video levels, minimum of 1 pixel interval.

4.2.2.1.4 Light Level (+) and (-) Outputs (Pins L and K respectively)

Level	This is another Binary output which may be used identically as Data (+)(-) above, thus providing two different thresholds to examine the video.

With jumper options it may be selected to latch when a pixel exceeds the threshold, and remain latched for an entire line or frame. See Section VI for a description of the jumper options available on this signal. It is to be received by a μA9637 line receiver or equivalent device meeting EIA-RS-422 specifications.

Pulse Period — Variable, depending on video levels and jumper options.

Pulse Width — Variable, depending on video levels and jumper options.

4.2.2.1.5 GCLK (+) and (-) Outputs (Pins M and N respectively)

Level — This is the primary clock output and may be selected to be continuous, or gated off during retrace intervals. See Table I "S1 switch settings" for options available. The signal is to be received by a μA9637 line receiver or equivalent device meeting EIA-RS-422 specifications.

Pulse Rate — 0.25 -5 MHz

Pulse Width — Adjustable 100-300 ns by means of clock pulse width control on controller A4 P/C board. (Negative Pulse.)

4.2.2.1.6 FEN (+) and (-) Outputs (Pins P and U respectively)

Level — This is the Frame Enable Signal which goes logically true at the beginning of pixel 1 of line 1 and false at the end of pixel 100 of line 100. The signal is to be received by a μA9637 line receiver or equivalent device meeting EIA-RS-422 specifications.

Pulse Rate — Frame Rate, 25-500 per second

Pulse Width — 100 line intervals

4.2.2.1.7 ESTART (+) and (-) Inputs (Pins S and R respectively)

Level — This is the External Start input which will initiate the camera scan on user command. It is to be driven with a μA9638 line transmitter or equivalent device meeting EIA-RS-422 specifications.

Note: Data contained in lines 1 and 100 of each frame is invalid when the system is operated in external start mode.

Pulse Rate	Frame Rate, synchronized with FEN or (MØ•EOF). See Timing Diagram, Figure 9.
Pulse Width	Two pixel intervals minimum. See Timing Diagram, Figure 9.

Note: Data contained in lines 1 and 100 of each frame is invalid when the system is operated in external start mode.

4.2.2.2 Data B Connector

The Data B Connector contains signals in addition to those in the Data A Connector that are useful in synchronizing the users system, re-referencing the differential video output, and master-slaving several cameras. Up to 100 feet of Belden 8774 cable may be used, and shields should be connected to the connector shells only. See Figure 28.

4.2.2.2.1 LEN (+) and (-) Outputs (Pins B and C respectively)

Level	This is the Line Enable signal which indicates the beginning and end of valid video for each line. It goes logically true at the beginning of pixel 1, and false at the end of pixel 100. It is to be received by a μA9637 line receiver or equivalent device meeting EIA-RS-422 specifications.
Pulse Rate	Line Rate
Pulse Width	100 pixel periods

4.2.2.2.2 Analog and Signal Ground (Pins E and F respectively)

The Analog Ground connects to the power supply ground in the controller. It should be connected to the users signal ground. Shields in the Data B cable should be tied to the connector shell only. Belden type 8774 cable is recommended.

4.2.2.2.3 50 (+) and (-) Video Output (Pins G and H respectively)

This is the differential video output of the controller and is in parallel with the 75 ohm twinax output, therefore, only one of these outputs can be used, not both simultaneously. This output can drive up to 100 feet of Belden 8774 shielded cable and should be received by an analog line receiver

circuit like that used in the controller to receive the camera video. See Figure 10. Specifications are with 50 ohm termination and differential output.

Blank Level	Adjustable +0.2 to -2 volts. Drift 0.5mv/°C.
Dark Level	Adjustable +0.2 to -2 volts. Drift 0.5mv/°C.
Saturation Level	Adjustable to +2 volts above dark level.
Dynamic Range	≥ 200:1
Random Noise	≤ 10 mv p-p
Coherent Noise	≤ 100 mv p-p
Data Rate	0.25 -5 MHz
Settling Time	< 50 ns to 95% of saturation level.

4.2.2.2.4 Digital Ground (Pins J and T)

This is the return for digital signals in the Data B connector.

4.2.2.2.5 RE-REF (+) and (-) Output (Pins K and L respectively)

Level	This signal can be used to DC restore the 50 or 75 ohm analog video at the far end of a cable, thus removing any baseline drift due to cable characteristic changes from temperature and humidity. It goes logically true at the end of pixel 100 of each line, and false two pixel intervals before pixel 1 of each line. It is to be received by a μA9637 line receiver or equivalent device meeting EIA-RS-422.
Pulse Rate	Line Rate
Pulse Width	3-15 pixel intervals set by retrace counter. If system is in external start mode, this signal will remain true after the end of a frame until a start command initiates a new scan.

4.2.2.2.6 HCLK (+) and (-) Output (Pins M and N respectively)

Level	This is the primary continuous running clock output from the system. It is to be received by a μA9637

line receiver or equivalent device meeting EIA-RS-422 specifications.

Pulse Rate	0.25 -5 MHz
Pulse Width	100-300 ns adjustable

4.2.2.2.7 MØ•EOF (+) and (-) Outputs (Pins P and U respectively)

Level	This signal can be used to synchronize multiple cameras, and/or as a flag for the External Start Signal (4.2.2.1.7). The external logic required to use the MØ•EOF signal for multiple camera synchronization is shown in Figure 29. NOTE: Controllers with serial nos. 78083 through 78091 have the M2 signal as this output. See Section 6 for changes required on these units to change to MØ • EOF output.
Pulse Rate	Frame Rate
Pulse Width	2 pixel periods minimum

4.2.2.3 Camera Connector

The controller camera connector is plug to plug compatible with the MC520 camera which may be connected to it by a length of cable determined by the following formula:

$$\text{Length} = \left[\frac{227}{\text{FMHz}} - 16\right] \text{ feet or 75 feet,}$$

whichever is less. FMHz is the maximum data rate used. Recommended cable type is Belden 8774, and an 8-foot length, with connectors installed, is supplied with the system.

4.2.2.3.1 Video (+) and Video (-) Inputs (Pins G and H respectively)
Specifications are at output of line receiver on TP-1 of A6 P/C board.

Saturated Light Level	2 volts p-p AC coupled, averaging around dark level.

Dark Level	+3 volts nominal
Dynamic Range	≥ 200:1
Random Noise	≤ 10 mv p-p
Coherent Noise	≤ 200 mv p-p
Scanning Rate	0.25 -5MHz
Settling Time	≤ 120 ns to 95% of saturation level
DC Restoration	Provided by controller video processing.

4.2.2.3.2 MCLK (+) and (-) Output (Pins M and N respectively)

Level	Master "X" Clock from controller to camera, received by a μA9637 line receiver, with 100 ohm termination in camera.
Pulse Rate	Adjustable 0.25 -5 MHz.
Pulse Width	Adjustable 100 ns to 300 ns

4.2.2.3.3 MIC (+) and (-) Output (Pins P and U respectively)

Level	Master "Y" Clock from controller to camera, received by a μA9637 line receiver, with 100 ohm termination in camera.
Pulse Rate	Line Rate
Pulse Width	Adjustable 3-15 pixel intervals by retrace counter in controller. Minimum count is determined by: Count Min. = 2(FMHz +1) where FMHz is maximum data rate used. For 5MHz count will be 2(5+1) = 12 minimum. See Table II for Counter Switch (S2) settings.

4.2.2.3.4 CCLK (+) and (-) Input (Pins B and C respectively)

Level	This is the Master Clock from the camera which is used to synchronize the controller to eliminate cable propagation delay differences. It is received by a μA9637 line receiver, and a 100 ohm termination is provided in the controller.
Pulse Rate	Adjustable 0.25 -5 MHz. (Clock Frequency Adjust)
Pulse Width	Adjustable 100-300 ns. (Clock Pulse Width Adjust)

4.2.2.3.5 EOF (+) and (-) Input (Pins K and L respectively)

Level	This is the End of Frame Signal from the camera which is used to Frame synchronize the controller. It is received by a μA9637 line receiver, and a 100 ohm termination is provided in the controller.
Pulse Rate	Frame Rate, 25-500 per second.
Pulse Width	One line interval (True during line 100.)

4.2.2.3.6 +5 Volts and Digital Ground (Pins T and J respectively)

The controller will supply camera power plus an additional 4.0 amperes to spare card positions A1 through A3 for user circuits.

4.2.2.3.7 +15 Volts (Pin E)

The controller will supply camera power plus an additional 1.0 ampere to spare card positions A1 through A3 for user circuits.

4.2.2.3.8 -15 Volts and Analog Ground (Pins R and S respectively)

The controller will supply camera power plus an additional 1.0 ampere to spare card positions A1 through A3 for user circuits.

4.3 ENVIRONMENTAL

4.3.1 Temperature

Operating Ambient	0 to +50°C
Storage	-20 to +100°C

4.3.2 Humidity

90% R.H. Non-Condensing

4.4 ADJUSTMENTS

A4 - PC board	R-Clock Frequency Adjust (R18), C-Clock Frequency Adjust (C1), Clock Pulse Width Adjust (R21), Int./Ext. Select (S1), Retrace Count (S2).
A6 - PC board	Receiver R Balance (R11), Receiver C Balance (C3), Receiver C Fine Balance (C12), Receiver Gain Adjust (R33), Y Sweep Amplitude Adjust (R123), X Sweep Amplitude Adjust (R120), Odd/Even Gain Balance (R52), Odd/Even Offset Balance (R50), Light Level Threshold (R137), Data Threshold (R141), Dark Level Adjust (R61), Blank Level Adjust (R9), Blank Level Balance (R62), Transmit Gain Adjust (R165), Transmit Balance (R150), Odd Pulse Width Adjust (R2), Even Pulse Width Adjust (R4).

4.5 P/C BOARDS

Digital Board - A4

Analog Board - A6

A/D Option P & S Board - A5

Interconnect Board

SECTION V

DETERMINATION OF OPTICAL, ILLUMINATION, AND MOUNTING REQUIREMENTS

5.1 OPTICAL RELATIONSHIPS

5.1.1 Field of View (F)

Field of View is defined as the length of the array side imaged onto the object plane. Since the array is square, this length will be identical in both the X and Y axes. For a size measurement, the field of view will be the maximum size of the part plus an alignment tolerance.

5.1.2 Magnification (M)

Magnification is the ratio of the field of view to the length of the array:

$$M = \frac{F}{AL}$$

where F is the field of view, and AL is the array length = 0.24 inch (0.60 cm) in both X and Y axes.

5.1.3 Static Resolution (RS)

Static resolution is defined as the array element spacing imaged onto the object plane.

$$RS = M \times ES$$

where M is the magnification, and ES is the element spacing = 2.4 mils (60 μm).

Static resolution is the smallest detectable change in the object dimensions, with the object stationary within the field of view.

For a measurement which includes both sides of an object, the best resolution is generally considered to be $\pm$ RS.

For a given geometrical relationship the resolution is fixed, but the accuracy depends on:

Image sharpness

Contrast
Vibration or movement of the object
Light level
Threshold setting and other related parameters.

5.1.4 Dynamic Resolution (RD)

When the object to be measured is moving in the field of view, the resolution is the static resolution (SR), plus a dynamic component equal to the distance the object moves during the time it is scanned.

For a measurement which includes both sides of an object the worst case dynamic resolution will be:

$$RD = \pm \left(RS + \frac{VxT}{2} \right)$$

where: RS = Static resolution
V = Average velocity of measured part during T
T = Time to scan part.

The dynamic resolution will be different in the X and Y axes, since Y axis scan time is 100 times the X axis scan time. Therefore, the smallest dimension of the moving object to be measured should be scanned in the X axis of the 100 x 100 sensor to obtain greatest measurement accuracy.

5.1.5 Working Distance (D)

The distance from the front of the camera lens to the object plane is defined as working distance. In general, the larger the working distance the more stable the measurement system. With greater working distances, movement of the object along the camera line-of-sight has less effect on magnification, consequently, calibration will hold for greater variations in this distance.

A longer working distance also means a narrower angular field, reduced geometrical distortion, and better lighting uniformity. Figure 11 shows working distance versus object magnification for standard "C" mount lenses.

5.1.6 Depth of Field

Depth of field is defined as the distance an object may move on the Z axis and still maintain a sharp image. Figure 12 shows depth of field versus magnification versus f-stop.

When objects are expected to move in the Z axis, the camera lens should be "stopped down" to increase the depth of field and maintain focus. This reduction in lens opening requires increasing the exposure by a factor of two for every increase in f-number. This is linear so that the depth of field at f/16 is 8 times that at f/2.

5.1.7 Optical Determination Example

At a working distance of 20", it is required to measure the dimensions of a rectangular plate 0.96" x 2.18" with an accuracy of $\pm$ 2.5%. The plate is moving in the Y direction of scan at 10 inches/second. For best measurement accuracy the 0.96" dimension will be scanned in the X direction and the 2.18" dimension in the Y direction.

The field of view must be 2.18" plus an alignment tolerance which we will choose as 10% = 2.18 + 0.218 = 2.4"

The magnification will then be:

$$M = \frac{F}{AL} = \frac{2.4"}{0.24"} = 10$$

The resolution in the X axis will be the static resolution since the part has no motion in that direction:

$$RS = \pm (M \times ES) = \pm (10 \times 0.0024) = \pm\ 0.024"$$

The measurement accuracy will then be 0.96" $\pm$ 0.024", or 0.96" $\pm$ 2.5%.

In the Y direction the dynamic resolution will be:

$$RD = \pm \left(M \times ES + \frac{V \times T}{2}\right) = \pm \left(10 \times 0.0024" + \frac{10 \times T}{2}\right)$$

$$= \pm\ (0.024" + 5T)$$

It is required that RD be $\pm$ 2.5% of 2.18" or $\pm$ 0.0545"

so that:

$$\pm (0.024 + 5T) \leq \pm 0.0545$$

or $5T \leq 0.0305"$

$T \leq 0.0061$ sec.

Where T is the time required to scan the 2.18" dimension of the part.

To determine the camera scan rate we first find the number of lines required to scan the 2.18" dimension:

$$\text{No. of Scan Lines} = \frac{2.18"}{M \times ES} = \frac{2.18}{0.024} = 91$$

we must then scan 91 lines in 6.1 ms or less. This is equivalent to 91 lines x 100 pixels = 9100 pixels in this time, which gives a scan rate of:

$$\text{Camera Scan Rate} \approx \frac{9100 \text{ pixels}}{6.1 \text{ ms}} \approx 1.5 \text{ MHz}, \approx 150 \text{ frames/second}$$

From Figure 11, for a magnification of 10 and working distance of 20", a 50 mm focal length "C" mount lens is required with a lens extension tube of 50 mm/10 = 5 mm (0.20").

Illumination tests are then run on the 0.96" x 2.18" part at 20" working distance, and, for purposes of this example, it is assumed an f/5.6 lens opening is required.

From Figure 12, the depth of field for f/5.6 and magnification of 10 will be 2.7".

5.2 ILLUMINATION REQUIREMENTS

To obtain a useful signal from the MC 520 camera, a certain exposure of the sensor element is required. Since exposure is defined as the light intensity on the sensor (μwatt/cm^2) multiplied by the frame scan time (sec.), the required light intensity is directly proportional to the frame scan rate. Although light intensity required on the sensor is well defined, only a small percentage of the light output from a typical light source actually illuminates the sensor. Therefore, in choosing a suitable light source, factors such as f-number, magnification, lighting arrangements, and surface condition of the object, i.e. light, dark, diffuse or specular, must be considered together with sensor sensitivity and scan rate.

Rear illumination is preferred where possible because less energy is required.

There are so many variables that no simple formula can be given. For many applications one of several available Reticon illumination sources will meet the users requirements. A complete analysis of the static, dynamic, and sensitivity factors is required to determine the best approach.

5.2.1 Array Sensitivity Characteristics

Figure 7 shows the RA-100 x 100 typical illumination characteristics, indicating the excellent sensitivity, linearity, and dynamic range obtained.

5.2.2 Array Blooming Characteristics

Figure 8 shows the RA-100 x 100 array blooming characteristics. These measurements were made by illuminating a spot in the center of the array covering an area of approximately 10 x 10 pixels. A line approximately 15 lines outside of the illuminated area is examined to determine the worst case effect of the charge "spillover" due to the excess light above saturation level within the illuminated area. This is expressed in a percentage of the actual photosensor saturation. For example, if the 10 x 10 pixel area is illuminated at 2X the photodiode saturation level, the blooming will typically be 5%, meaning that a photodiode outside the illuminated area can produce an error signal of 5% of its saturated output.

5.2.3 Camera Mounting

The MC 520 camera is supplied with four 6-32 drilled and tapped holes in its case, as well as a single 1/4-20 threaded tripod mounting hole.

It is recommended that for permanent installation the four 6-32 holes be used to securely fix the camera to its mounting position. The tripod mounting is provided for temporary or movable mounting only.

Figure 2 details the MC 520 mounting hole dimensions. It is best to mount the camera so that it has some freedom of movement along the Z axis for focus and magnification settings.

If precise alignment is required between the camera field and an object whose position is fixed, the mounting arrangement should also allow for transverse movement of the camera.

SECTION VI

INSTALLATION AND ADJUSTMENT

6.1 GENERAL

Before mounting the camera or using the controller, internal electronic adjustments may be required to suit the particular user's application.

This section details both electronic and optical adjustments necessary to provide appropriate operating characteristics for a typical industrial environment.

6.2 MC520 CAMERA ELECTRONIC ADJUSTMENT

Camera adjustments have been set at the factory; however, certain adjustments, as noted, change somewhat with scan rate, and it may be desirable to optimize these at the rate required by the user. Also complete readjustment may be required if the camera to controller connecting cable length is changed, or the camera is used with a controller other than that for which the camera was originally adjusted, or if the array or other components are replaced.

The following paragraphs describe the adjustment procedures necessary to bring the camera into factory calibration. It is assumed that no malfunctions exist in the camera or controller during the following procedures.

Open the camera as described in 9.16, and remove the screw covering the gain adjustment on the camera rear panel. (See Figure 2.)

During the adjustment procedures refer to Drawings 010-0222, 010-0242, 010-0223, and Figure 2, for test point and adjustment locations.

6.2.1 Initial Coarse Adjustment

a. Set the controller switch S1 on the A4 board for Internal Clock and Start (See Table I).

b. Set the controller switch S2 on the A4 board for a count of three (See Table II).

c. Set the controller frequency for 500 KHz (See 6.3.4).

d. Set the voltage at TP6 on the camera A2 board to nominally 12.60 volts by means of the V_{BUF} adjustment, R23.

e. Set the voltage at TP8 on the camera A2 board to 10.50 volts by means of the V_{BB} adustment, R21.

f. Set the voltage at TP4 on the camera A2 board to 4.25 volts by means of the V_Q adjustment, R20.

g. Set the voltage at TP3 and TP4 on the camera A2 board to be equal within 10 millivolts by means of the V_Q Balance adjustment, R19.

h. Readjust the V_Q adjustment, R20, so that the voltage at TP4 on the camera A2 board will again be 4.25 volts.

i. Set the gain balance adjustment, R33, on the camera A1 board to mid-travel (12.5 turns from end).

j. Set the LR/LT control, R14, on the camera A1 board fully counterclockwise.

k. Set the gain adjustment, R20, through the camera rear panel to mid-travel (1/2 turn from end).

6.2.2 Final Adjustment

Where applicable, observe the camera video with an oscilloscope at the center BNC jack on the camera rear panel. Synchronize the oscilloscope on the right BNC, FSYN, signal.

6.2.2.1 ØY and Gain Balance Adjustment

After initial adjustment, the camera video signal may have the appearance of the upper trace in Photograph 1. When array is not illuminated the low frequency is video line offset, and the high frequency is pixel offset. Balance out the pixel offset by means of the Gain Balance adjustment, R33, on the camera A1 board until the video is as shown in the lower trace of Photograph 1.

This leaves the line offset as shown in the upper trace of Photograph 2; balance this out by means of the ØY Balance control, C34, on the camera A1 board until the video is as shown in the lower trace of Photograph 2.

The ØY Balance adjustment changes somewhat with camera scan rate, and, after all final adjustments are complete at 500 KHz, it may be desirable to optimize the ØY adjustment at the users chosen scan rate if required.

Note: Gain Balance and Øy adjustments are to be made with array in total darkness.

6.2.2.2 LR/LT Adjustment

Rotate the LR/LT control, R14, on the camera A1 board until the video signal has the appearance of the upper trace of Photograph 3, showing unbalance between the Array odd and even BBD registers. Turn R14 counter-clockwise until the unbalance just disappears, and then another 1/2 turn. This adjustment is performed with array in total darkness. This adjustment changes somewhat with camera scan rate, and after all final adjustments are complete at 500 KHz, it may be desirable to optimize the LR/LT adjustment at the users chosen scan rate for minumum video blooming.

6.2.2.3 V_Q Adjustment

Observe the camera video on TP2 and TP3 of the camera A1 board (with a x10, 10 pf probe). The waveforms should appear as in the upper and lower trace respectively of Photograph 4. Set the peak-to-peak amplitude of either waveform to 1.1 volts by means of the V_Q control, R20, on the camera A2 board. Both waveforms should then have the same approximate p-p amplitude. This adjustment is performed with array in total darkness.

Note: On cameras with Serial Numbers 78038 thru 78045 TP2 and TP3 do not exist. Observe directly at pins 12 and 13 of device U4, the 100x100 array.

6.2.2.4 Gain Adjustment

Remove the camera lens and apply a piece of black masking tape, with a 1/16-inch hole punched in it, over the photosensor window. The 1/16-inch hole should half overlap the left edge of the light sensitive area about midway between the top and bottom of the monitor presentation as shown in Photograph 5. The black masking tape should cover the entire photosensitive area except where the 1/16-inch hole is punched.

Leave the lens off the camera, and illuminate the photosensor area with a steady state light source such as a battery operated lantern or flashlight, or an incandescent lamp operated from a dc power supply. This should be done in semi-darkness so that ambient illumination will be minimized. Move the light source toward or away from the camera until the output video signal from the camera due to the illumination through the 1/16-inch hole is at approximately 90% of saturation. The oscilloscope presentation should appear as in the upper trace of Photograph 6.

Without changing the illumination on the photosensor, adjust the video Gain, R20, through the rear panel adjustment hole, until the peak-to-peak signal amplitude is approximately 2 volts.

6.2.2.5 V_{BUF} Adjustment

Increase the light intensity, used in 6.2.2.4 above, until blooming causes 100% saturation of the pixels adjacent to the 1/16-inch light spot as

shown in the lower trace of Photograph 6 and upper trace of Photograph 7.

Adjust the V_{BUF} control, R23, on the camera A2 board to minimize the blooming as shown in the lower trace of Photograph 7.

Check TP6 on the A2 board for a dc level of +12 to +13 volts.

The V_{BUF} adjustment changes somewhat with camera scan rate; therefore, after all final adjustments are complete at 500 KHz, it may be desirable to optimize the V_{BUF} adjustment at the users chosen scan rate for minimum blooming.

6.2.2.6 V_{BB} Adjustment

While observing the video waveform shown in the lower trace of Photograph 7 with the oscilloscope, use the delayed sweep to isolate a single video line in the middle of the oversaturated light spot as shown in the upper trace of Photograph 8.

Adjust the V_{BB} control, R21, on the camera A2 board until the last pixel in the line (D1 in the Timing Diagram of Figure 9) is at approximately 50% of saturation level as shown in the upper trace of Photograph 8.

Now adjust the V_{BB} control until the D1 pixel reduces to the same level as the dark level and appears as shown in the lower trace of Photograph 8.

Check the dc voltage at TP8 on the camera A2 board for +10.5 to +11 volts.

Recheck the V_Q setting per 6.2.2.3 and readjust if necessary.

6.2.2.7 VQ and Gain Balance Adjustment

Reduce the light intensity of 6.2.2.6 until the video signal is again at approximately 90% saturation within the area of the illuminated spot. Adjust the video Gain control, R20, through the rear panel adjustment hole, until the peak-to-peak amplitude is again 2 volts, if necessary.

Observe a single line on the oscilloscope as in 6.2.2.6, which may show both dark and light level offset as shown in the upper trace of Photograph 9.

Adjust the V_Q Balance control, R19, on the camera A2 board until the dark level offset is balanced as shown in the lower trace of Photograph 9 and upper trace of Photograph 10.

Adjust the Gain Balance control, R33, on the camera A1 board until the light level offset is balanced.

Go alternately between the R19 and R33 adjustments until both light and dark level offset is balanced as shown in the lower trace of Photograph 10.

6.2.2.8 V_{IRIS} Balance

After all other camera adjustments have been made, observe TP1 on the camera A2 P/C board with an oscilloscope. The waveform will appear as in the upper trace of Photograph 11 if the circuit is unbalanced. Adjust the V_{IRIS} zero control, R5, on the A2 board to balance out the square wave as shown in the lower trace of Photograph 11. The adjustment is performed with array in total darkness.

6.2.2.9 Cleaning Array Window

Paragraph 6.2.2.8 concludes calibration and adjustment of the MC520 camera. Leave the black masking tape over the array if the controller is to be adjusted. If not, remove the tape and carefully clean the array window with lens tissue moistened with alcohol.

Close the camera case.

6.3 RS520 CONTROLLER ELECTRONIC ADJUSTMENT

The RS520 Controller has several adjustments which are factory set, and should not require readjustment unless the camera to controller connecting cable length is changed, or electronic components age or are replaced. Other adjustments may be varied to suit a particular users requirements. Both factory and user adjustments, as well as jumper options, will be described in the following paragraphs.

Refer to Drawings 010-0224, 010-0225, and Figure 27 for adjustment and test point locations.

6.3.1 Power Supply Adjustment

The controller power supply generates ± 15% volts and +5 volts which are adjustable. Although the system components will operate with the voltages within ± 5% of their nominal values, they should be set to within 100 millivolts of the nominal values. Adjustment locations and the appropriate terminals for measuring these voltages are shown in Figure 27.

Note that the supplies are overvoltage protected, and should adjustment exceed these upper voltage limits the supply will "crowbar" into

a current foldback condition. To recover from this, return the adjustment to a value below the overvoltage limit and turn power off and on to restore operation to normal. Power supply adjustments should be performed before adjusting either the MC520 or RS520.

6.3.2 Controller Clock and Start Mode Selection

Data rate and scan initiation may be determined by either controller internal logic, or externally by user supplied signals.

If internal Clock and Start modes are selected, scans are automatically initiated, and data rate is determined by the internal clock generator. Rate can be continuously adjusted from 500 KHz to 5 MHz as described in 6.3.4.

If external mode is selected the user must supply clock and start pulses meeting the specifications of Section IV, at the desired data and frame rate.

The external start pulses may be entered asynchronously after the (MØ•EOF) signal goes true, see Timing Diagram, Figure 9.

It should be remembered that although initiation of a new scan can be delayed by delay of the External Start pulse, light integration is continuous, and, therefore, light sensitivity for the delayed frame will increase proportionately as a result of the effective decrease in frame rate.

Internal Clock and/or Start mode selection is determined by switch bank S1 on the controller A4 P/C board. See Table I to determine the desired settings.

6.3.2.1 GCLK Mode Selection

The GCLK output may be selected to be continuous or gated as desired. Controller switch bank S1 on the A4 board determines the mode. See Table I for an explanation of the modes available and the switch settings to obtain them.

6.3.2.2 Master Slaving Multiple Cameras

Master-Slave synchronization of two cameras can be accomplished by means of the logic shown in Figure 29. More than two cameras can be synchronized by extension of this logic. With this logic in operation, each pixel of each line, and each line of each frame will occur simultaneously in the synchronized cameras.

Note: Data contained in lines 1 and 100 of each frame is invalid when the system is operated in external start mode.

The notes of Figure 29 explain how the logic is connected to the controllers, and what clock and start mode is required.

If External Start mode is desired, the controller ESTART inputs should be driven in parallel from the external start pulse source.
Note: Data contained in lines 1 and 100 of each frame is invalid when the system is operated in external start mode.

6.3.3 Retrace Count Selection

The Retrace Count determines the length of time used to transfer a video line into the BBD registers. The minimum time for a complete transfer is 2 microseconds. The Retrace Count must then be set for the number of pixel intervals whose sum is a minimum of 2 microseconds plus 2 additional intervals required for the "Fill and Spill Cycle". The minimum count required is described by the following formula:

$$\text{Retrace Count Minimum} = 2(\text{FMHz} + 1)$$

For example, if the pixel rate is 1.7 MHz, the minimum count required is $2(1.7 + 1) = 5.4$. Use the next highest integer, 6.

Although counts as high as 15 may be selected, video blooming will be minimized if the above formula is used.

The Retrace Count is selected by means of switch bank S2 on the controller A4 P/C board. See Table II for instructions to set this switch bank to a desired count.

Once set, the actual count can be observed on the oscilloscope by connecting one trace of the oscilloscope to TP1, and the second trace to TP2 on the A4 board. Signal waveforms will be similar to the upper and lower traces of Photograph 12. The upper trace is MCLK and the lower is M1. The length of time that M1 is true spans three MCLK intervals, therefore, the count is set for three in this example, which is the minimum count required for a pixel rate of 500 KHz.

The actual video blanking interval will be:

$$\text{Blanking Interval} = (\text{RTC} + 2)T$$

where RTC = Retrace Count, and T = Pixel Interval = $1/_{\text{FMHz}}$

6.3.4 Clock Frequency and Pulse Width Adjustment

The upper trace of Photograph 12 shows the MCLK waveform appearing at TP1 on the controller A4 board when the internal clock mode

is selected. The frequency of this pulse train can be adjusted from 0.5 to 5 MHz by means of the clock R and C controls, R18 and C1, on the controller A4 board. At the highest and lowest frequencies the R Control, R18, will be at an extreme end of adjustment, and fine control will be difficult. In these cases, the C Control, C1, will provide the fine adjustment needed.

Frequencies down to 0.25 MHz may be obtained by installing a user supplied padding capacitor in the optional C2 position on the A4 board.

The upper 5 MHz frequency can be obtained only if the MCLK pulse width is set for a maximum of 100 nanoseconds. Pulse width adjustment is provided by R21 on the A4 board, and may be set to any width from 100 to 300 nanoseconds, but should be less than 60% of the MCLK period.

With the setting at 100 nanoseconds the system will operate properly over the entire range of 0.25 to 5 MHz, and the only reason to increase this width is to provide a wider GCLK or HCLK output pulse to suit user requirements.

When External clock mode is selected (See Table I), the frequency of the pulse train at TP1 will be determined by the user supplied clock frequency. The pulse width will still be determined by the Pulse Width adjustment, R21.

Camera Scan rate is related to the Clock rate by the following formula:

$$\text{Scan Rate} = \frac{\text{FMHz} \times 10^4}{102 + \text{RTC}} \text{ , Frames Per Second}$$

where FMHz is clock rate, and RTC is Retrace Count.

If the minimum Retrace count is used at all clock frequencies, this formula reduces to:

$$\text{Scan Rate} = \frac{10^4}{\frac{104}{\text{FMHz}} + 2} \text{ , Frames Per Second}$$

For example at 5 MHz, scan rate would be $\frac{10^4}{\frac{104}{5} + 2} = 438.6$ Frames Per Second

6.3.5 Analog Line Receiver Common Mode and Gain Adjustment

The Analog Receiver Common Mode Balance is adjusted at the factory, and should not require readjustment unless components age or are changed.

The Gain adjustment sets the video level calibration for the entire camera/controller system and may require adjustment according to the users application.

6.3.5.1 Gain Adjustment

With the camera Gain adjusted as in 6.2.2.4, connect the camera to the controller and illuminate the photoarray with a light source (flashlite, lantern, etc.). Observe TP1 on the controller A6 board with the oscilloscope. The oscilloscope should be ac coupled as the video averages around a +3 volt dc level. Adjust the light source for almost light saturation as evidenced by flattening of the video waveform peaks.

Adjust the Receive Gain control, R33, until the peak-to-peak video at saturation is 2 volts.

This adjustment will be set again as part of overall calibration in 6.3.9.

6.3.5.2 Common Mode Balance (Factory Adjustment)

Remove P2 from the side of the controller A6 board, and insert another plug which connects both differential inputs in parallel to a square wave generator. The generator frequency is first set to 500 KHz and a peak-to-peak signal amplitude of 2 volts averaging around ground. This waveform is shown in the upper trace of Photograph 13.

Observe TP1 on the controller A6 board with the oscilloscope, which, if the circuit is unbalanced, may have a waveform similar to the lower trace of Photograph 13 and upper trace of Photograph 14. Adjust the R Balance control, R11, on the A6 board until the square wave is balanced out as shown in the lower trace of Photograph 14.

Increase the square wave frequency to 5 MHz, and maintain the 2 volt p-p amplitude averaging around ground as shown in the upper trace of Photograph 15. Again observe the signal at TP1 on the A6 board with the ac coupled oscilloscope. The waveform may be as shown in the lower trace of Photograph 15 and upper trace of Photograph 16.

Adjust the C Balance control, C3, and C Fine Balance control, C12, alternately until the unbalance is minimized as shown in the lower trace of Photograph 16.

6.3.6. Odd and Even Sample Pulse Width Adjustment

For operation over the entire clock range of 0.25 to 5 MHz, the Odd and Even sample pulse widths should be adjusted to 150 nanoseconds $^{+0}_{-10}$ nanoseconds.

At frequencies lower than 5 MHz, the widths may be increased with some small attendant increase in camera sensitivity. In any case, the widths should not be greater than the pixel period minus 50 nanoseconds nor less than 140 nanoseconds. Thus at 5 MHz clock rate, the maximum width should be (200 ns. -50 ns.) = 150 nanoseconds as stated above.

The pulse widths are adjusted by observing TP6 (Odd) and TP7 (Even) with the oscilloscope, as shown in the upper and lower traces, respectively, of Photograph 17. Adjust the Odd Pulse Width by means of R2, and the Even Pulse Width by means of R4, on the controller A6 board.

6.3.7 Sample-and-Hold Gain and Offset Balance Adjustment

Adjustment of the Sample and Hold Gain and Offset Balance is similar to the adjustment of the MC520 camera Gain and V_Q balance adjustment; therefore, the same light source as described in 6.2.2.4 is used, as well as the same Photographs.

With the MC520 camera connected to the controller, generate a light spot at 90% saturation as described in 6.2.2.4, and use delayed oscilloscope sweep to isolate a single video line in the center of the spot while observing TP2 on the controller A6 board with the ac coupled oscilloscope. The waveform may appear as in the upper trace of Photograph 9, but inverted. If the oscilloscope can invert the signal, do so to make the trace identical to Photograph 9.

Adjust the Offset Balance control, R50, on the A6 board until the dark level offset is balanced as shown in the lower trace of Photograph 9 and upper trace of Photograph 10.

Adjust the Gain Balance control, R52, also on the A6 board, until the light level offset is balanced.

Alternately adjust R50 and R52 until both dark and light level offset are balanced as shown in the lower trace of Photograph 10.

6.3.8 Dark Level and Blanking Level/Balance Adjustment

The Dark and Blank levels may be independently adjusted to suit the users requirements. Usually the Dark Level is set to zero volts, and Blanking Level to a value that causes video blanking during the retrace intervals.

The upper trace of Photograph 18 shows both Dark and Blanking Levels set to zero volts. The lower trace shows the Blanking Level negative by 400 millivolts with respect to the Dark Level.

To adjust the levels and their balance, put the camera in darkness and observe the video signal at the Z output BNC on the controller rear panel with the oscilloscope. The output should be terminated or unterminated as desired.

First adjust the Blanking Level to zero volts by means of the Blank Level adjust, R9, on the A6 board. The Dark Level will also change, but disregard this.

Next adjust the Dark Level to within 20-40 millivolts of zero volts, by means of R61 on the A6 board, as shown in the upper trace of Photograph 19.

Set the Retrace Count switch to 15 as described in Table II. The video may have a "tilt" during the blanking interval as shown in the upper trace of Photograph 19. Balance this out by means of the Blanking Balance control, R62, on the A6 board until the video appears as in the lower trace of Photograph 9.

After the Blanking Balance has been adjusted, reset the Retrace Count switch to 3, and readjust the Dark and Blanking Level controls to whatever voltages are desired within the Specification of Section IV. Always adjust the Blanking Level first, and Dark level second since the Blanking Level interacts with the Dark Level but not vice versa.

6.3.9 Transmit Gain and Balance Adjustment

With the camera in darkness, adjust the Dark and Blanking levels to zero volts as in 6.3.8 above, at the Z BNC jack. Balance the Analog Line Transmitter with the Transmit Balance control, R150, on the controller A6 P/C board. Adjust this control until both the (+) and (-) outputs on the 75 ohm Twinax connector, located on the controller rear panel, are at the same voltage. Each output (+) or (-) should then be within ±30 millivolts of ground potential.

Using the point light source described in 6.2.2.4, adjust intensity until 90% saturation level is reached at the Z BNC jack. Adjust the Analog Line Receiver Gain control, R33, until 90% saturation level is 2 volts peak positive video at this Z BNC. Then adjust the Transmit Gain control, R165, on the A6 board for 4 volts peak differential video across the 75 ohm Twinax connector without termination, or 2 volts peak with 75 ohm termination.

6.3.10 Data and Light Level Threshold Adjustment

The Data and Light Level Threshold comparison levels are on TP4 and TP3, respectively, of the controller A6 board. Additionally, the Data Threshold Level appears through a 10 Kilohm resistor on the Threshold BNC jack on the controller rear panel. This BNC jack must see a high impedance in order to have accurate measurements.

Both Data and Light Level Threshold values may be accurately set by comparison to the video signal on TP5 on the A6 board, or less accurately set (±30 millivolts) by comparison to the video signal on the unterminated Z output BNC jack.

The Light Level and Data Threshold levels are adjusted by means of R137 and R141, respectively, on the controller A6 board.

The upper trace of Photograph 20 shows four video lines at the edge of the light spot used for camera and controller adjustment, superimposed with the Data Threshold level. The lower trace shows the Binary Data output response at TP11 of the A6 board, as well as at the Data A I/O connector on the controller rear panel.

The Binary Light Level output response depends on jumper options as described in 6.3.15, and appears on TP10 as well as the Data A I/O connector.

Both Data and Light Level Thresholds can be used identically if proper jumpers are installed, thus providing for dual threshold examination of the video signal.

6.3.11 X and Y Sweep Amplitude Adjustment

The X and Y Sweep Amplitudes may be adjusted to any value from -2 to +2 volts unterminated, -1 to +1 volt terminated.

The upper and lower traces of Photograph 21 show the +2 and -2 volt X Sweep outputs, respectively, and Photograph 22 shows the same waveforms for the Y Sweep.

To adjust these outputs, observe the signal on the appropriate X or Y BNC jack on the controller rear panel, and adjust the X Amplitude by means of R120, and Y Amplitude by means of R123, on the A6 board. The controls will change the signal from minus, through zero, to plus levels, as they are rotated.

If desired, observe the raster generated by the sweeps on a monitor, and adjust the amplitudes for the required picture size.

6.3.12 Pixel Blanking Jumper Option

The first and last two pixels of each video line are slightly offset from the remainder of the line.

If desired, these may be blanked from the video signal by appropriate choice of jumpers W1 through W8 on the controller A4 board.

As received from the factory, jumpers W2, W3, W6, and W7 are installed as traces on the board. To blank the unwanted pixels, cut W2, W3, W6, and W7, and install jumper wires at W1, W4, W5, and W8. See Figure 30 for jumper locations on the A4 board.

6.3.13 Signal Selection Jumper Options

As received from the factory, jumpers W10, W11, W12, and W14 are installed as traces on the controller A4 P/C board.

These jumpers are located at the inputs to the digital line transmitters. If desired, these traces may be cut and wires run from any desired logic signal on the A4 board to any of these line transmitters, thus making them available at the controller Data A or Data B I/O connector.

On controllers with serial numbers from 78083 to 78091, jumper W10 should be cut and a wire run from pin 2 of device U15A to the jumper pad connected to pin 2 of device U20B. This brings out the (M0•EOF) signal to be used to master-slave multiple cameras, or synchronize the External Start mode as explained in 6.3.2 and 6.3.2.2.

6.3.14 Pixel Counter Jumper Options

Jumpers W15 through W30 are installed as traces on the controller A4 P/C board. These jumpers select the proper count for 100 pixels per each video line, and should not be modified by the user.

6.3.15 Light Level Jumper Options

The W1 through W7 jumpers on the controller A6 board provide for several modes of Light Level detection and presentation. Table III shows the jumper options and performance obtained with each.

6.4 USER I/O CABLE PREPARATION

User I/O cables connected to the controller Data A or Data B connector can be up to 100 feet long. It is recommended that the cables be prepared as shown in Figure 28, using Belden 8774 or equivalent shielded twisted pairs. Note that the shields are connected to chassis ground only, and that pairs have been assigned to specific pins in the connectors.

Note that the controller analog and digital output drivers have series RC networks for terminating and compensating for cable length. For cable lengths of up to 50 feet, the resistor termination provided will be adequate. For lengths greater than 50 feet the optional capacitors may improve rise and fall time response, and increasing the digital driver resistor values to 27 ohms from 2.7 ohms will reduce cable reflections. The value of the capacitors will be in the neighborhood of 680 pf, but should be determined by experimentation with the cable length installed.

6.4.1 D.C. Restoration of Video Output Signals

The 50 or 75 ohm differential video output signals from the controller may be used directly if short transmission cables are used. For long cables it may be desirable to dc restore the signal to eliminate any drift caused by cable characteristic changes due to temperature, humidity, etc. The digital output signal, REREF, may be used to implement dc restoration at the user end of the cable. This may be done with circuits similar to those used to dc restore the video signal from the camera in the controller. See "Principles of Operation", Section VIII, for a discussion of controller circuit operation, and contact Reticon for additional applications assistance with the users particular installation.

6.5 OPTICAL ADJUSTMENT

Before mounting the camera, electronic and optical adjustments may be required to suit the particular users application. The required adjustments are discussed in the following paragraphs.

6.5.1 Exposure Adjustment

Before camera position, magnification, and focus can be adjusted, the exposure must be set so that a proper video level may be obtained to locate the viewed object.

The effective exposure on the array is influenced by three factors:

1. Line scan time
2. Lens f-stop
3. Light Level

6.5.1.1 Line Scan Time

The required line scan time should be approximately known from the information presented in Section V. This may be set by either internally or externally generated start signals. See 6.3.2 and 6.3.4 for adjustments to select mode and data frequency, and relationship of frequency to line scan time.

6.5.1.2 Lens F-Stop Adjustment

It is assumed that the required f-stop has been determined from Section V. Set the lens to this value before proceeding with adjustments.

6.5.1.3 Light Level Adjustments

With the line scan time and lens f-stop set per previous determinations, observe the video output on the Z BNC jack and synchronize the oscilloscope on the Sync BNC jack. Adjust the oscilloscope sweep to view one complete camera frame.

With the object to be scanned in its required viewing position, and the camera positioned at the required working distance as determined from Section V, adjust the position of the light source for best illumination uniformity as observed on the oscilloscope display. Reduce the light intensity as necessary to observe this uniformity without saturation of the video signal. When the correct position is found, lock the light source into place.

6.5.2 Video Dark and Blank Level Adjustment

Before proceeding with object centering, adjust the video Dark and Blanking levels to zero volts as described in 6.3.8.

6.5.3 Object Centering

With the camera mounted in its required operating position with the light source, and at proper working distance and lens opening, observe a single video scan with the oscilloscope on the Z BNC jack and synchronized on the Sync BNC jack.

Adjust the camera until the object to be scanned is centered in the scan as determined by its being centered in the video pattern. If a video monitor is connected to the X,Y, and Z BNC jacks, the object can be centered by watching the monitor presentation.

It is assumed that freedom of movement has been allowed in those axes which require precise adjustment.

6.5.4 Focus Adjustment

With electrical adjustments, camera, and light source positions fixed as described in previous paragraphs, final mechanical adjustments can be performed to achieve proper focus and magnification. Magnification and focus are interacting adjustments, and may require several trials to determine best settings. The camera working distance and lens f-stop settings have been set from previous determinations. Verify that the proper lens, and extention tube if required, is in fact installed, and set the lens to its minimum f-stop number (maximum opening) for the following adjustments:

1. Observe the controller Z output BNC jack with the oscilloscope, and synchronize on the Sync BNC jack.

   Adjust the time base so a well defined object edge is in view and the photodiodes in the transition are discernable.

2. As the array scans across the object, adjust the light intensity to obtain a video level slightly less than saturation.

3. Focus the lens by adjusting the focus ring, or extension tube length, while observing the video signal as the scan crosses the object edge. As the point of best focus is reached, the video signal will be seen to encompass the least number of array photodiodes in the edge transition. Leave the lens focused at the best point, and return the lens f-stop to the final measurement position.

If a video monitor is available, best focus can be determined by observing the raster display.

6.5.5 Threshold Adjustment

Before magnification can be accurately checked, the Data Threshold must be set. This level is set at the factory at approximately 60% of the video saturation level, but for many applications another level may be more desirable.

If the measured object is being lighted from the rear, the distinction between light and dark video is greatest, so that more tolerance is allowed for threshold setting. In this case, factory adjustment may be acceptable. However, if the object is front lighted, it is possible the separation between light and dark video signals may be small, and threshold setting critical.

In either case, front or back lighted, the thresholds may be readjusted by observing the video and threshold levels on the oscilloscope and adjusting the Data threshold potentiometer, R141, on the controller A6 board, until the level is at mid-point between the highest and lowest video levels seen in the video frame.

The Light Level Threshold is a second threshold which may be adjusted independently of the Data Threshold. The Light Level Threshold is set at the factory to approximately 80% of the video saturation level. This level may be adjusted by means of R137 on the controller A6 board. Binary output response of the Light Level Threshold comparison may be set to several modes by means of jumper options on the A6 board. See Table III for a description of these options.

6.5.6 Magnification Adjustment

Once focus and threshold have been set, magnification can be checked by counting the number of array diodes within a known dimension of the scanned object. If the camera is connected to a Reticon controller, this check is easily accomplished by setting the controller to count and display the number of photodiodes within a known dimension.

Without a Reticon controller, observe the Data binary output on TP11 of the A6 board on one trace of the oscilloscope, and the MCLK signal on TP1 of the A4 board on the second trace, while synchronizing on the Sync BNC jack.

While observing the Data and MCLK signals, count the number of MCLK pulses within the true level of the Data signal defining a known dimension of the scanned object.

Magnification is then:

$$M = KD/(ES \times NC)$$

where: M = Magnification

KD = Known Dimension

ES = Array Element Spacing = 2.4 mils (60μm)

NC = Number of Clock Pulses within Known Dimension

If the magnification so determined does not meet requirements, change the camera Z axis position and repeat focus/magnification adjustments as many times as necessary to bring it into required value. Reducing the working distance increases the number of clocks, and increasing it decreases the number of clock pulses within the known dimension.

Once light level, focus, and magnification have been properly set, camera and light source may be permanently locked into position.

SECTION VII

PRINCIPLES OF OPERATION
MC 520 CAMERA

7.1 INTRODUCTION

This section contains an overall functional description of the MC 520 camera electronics which are contained on three printed circuit cards within the camera housing. See Figure 2 for P/C card location, Figure 3 for a Simplified Electronics Diagram, and Figure 26 for a logic flow diagram.

The P/C cards are designated A1 through A3, and their operation will be described in conjunction with the RA-100 x 100 matrix array.

7.2 RA-100 x 100 ARRAY

The RA-100 x 100 matrix array is mounted on the A1 board. It is a monolithic photodiode array of 10,000 pixels arranged in a 100 x 100 matrix on a 2.4 mil (60μm) center-to-center spacing. Referring to the array schematic diagram Figure 13, the Dynamic Shift Register has 100 parallel output lines which are sequentially selected as the ØY1 and ØY2 clock lines are complemented. Each of these 100 output lines connect to an N channel MOS switch. The gates of these switches connect to input line LO for the odd numbered lines, and LE for the even. In the MC 520 camera, the LE and LO inputs are connected to VDD so that the switches are continuously on, and may be considered a short circuit. Following the schematic further, then, shows each of the 100 output lines from the Dynamic Shift Register connecting to the gates of 100 MOS switches, and each of these switches in turn connect between a photodiode sensor and a vertical "video line". Therefore, when an output line from the Dynamic Shift Register is logically true, the 100 photodiodes for that line are connected to 100 "video lines". Fifty of these lines exit the array toward the top of the schematic drawing, and 50 toward the bottom (Figure 13), connecting in both cases to an MOS transistor whose gate is connected to the input line VBUFF. These transistors eliminate fixed pattern noise effects from transistor threshold differences. The output of these "Buffer" transistors in turn connect to two MOS switches, one between the "video line" and VDD, whose gate connects to the input line LR, and another between the "video line" and the BBD X transport register, whose gate connects to the LT input line. The 50 video lines toward the top of the schematic connect thru the "LT" transistor to the EVEN BBD X transport, and the 50 toward the bottom to the ODD BBD X transport. These "transports" are Analog Bucket Brigade Shift Registers which accept information from the 100 pixels in a line and subsequently

shift them out serially as the ØX1 and ØX2 clock lines are complemented. The LR and LT (Line Reset and Line Transfer) inputs are synchronized such that the data from the 100 pixels of a selected line are transferred into the "X Transports", and then the "video lines" are reset to remove any residual charge and prepare for the next sequential line of 100 pixels.

Before proceeding, note that another group of MOS switches connected between VDD and the Dynamic Shift Register output lines (through the LE and LO switches) having their gates connected to input line FR, are not used in the MC 520 camera, as the FR input line is connected to ground, thus turning off these switches.

Following transfer of 100 pixels into the X Transport Registers, the video is shifted serially to the Odd and Even video outputs as the ØX1 and ØX2 clocks are complemented. An off chip resistor to ground on each of the video outputs forms a low impedance source follower to extract the video voltages. The Odd and Even Video outputs are summed off chip to produce a single serial output of 100 pixel intervals for each of 100 lines, for a total of 10,000 pixel intervals per frame.

The X BBD Transport stages have a "tetrode" transistor connected between each "bucket." The gates of these transistors connect to VBB, and the transistor provides high efficiency transfer of charge between each "bucket." Additionally, each BBD output has a transistor connected between the output and RD, with the gate connected to VR1 or VR2. These transistors are synchronized such that when pixel information is from the Odd BBD, the Even BBD output is reset and vice versa.

Each of the 100 lines from the Dynamic Shift Register, except line 100, is connected to the input of a 99 input "NOR" gate. When line 100 is reached, the "NOR" gate is enabled which reloads a logical "1" into the shift register and produces the EOF output from the array which is subsequently used to frame synchronize the camera and controller. Following line 100 , the Dynamic Shift Register advances to line 1. The Y start input is grounded in the camera, allowing this automatic advance to line 1 when ØY1 and ØY2 complement. The controller may delay this advance by delaying the ØY1 and ØY2 clocks until an external start command is received from the user. See Section VIII for a description of External Start.

7.3 ARRAY BOARD-A1

Refer to the A1 Board Functional Diagram, Figure 14, during the following discussion.

Inverters U1A,B, U2A,B, U3A,B, and their input bias networks R1-R6 and C1-C6 provide TTL to MOS Level Translation between the TTL

signals on P3 and the MOS signals on the array, U4. Resistors R15-R20 with the intrinsic capacitance of the on-chip transistors provide "tailoring" the signal rise and fall times for optimum performance. The variable capacitor C34 (ØYBAL.) allows balancing out any odd/even line fixed pattern noise, while R14(LR/LT Adj.) provides adjustment of minimum pixel fixed pattern noise due to array transistor threshold variations.

All MOS logic levels at the array, U4, swing nominally between +1volt and +14 volts.

During video line 100 the $\overline{EOF}$ signal on pin 2 of U4 goes false (+1 volt). The on-chip device is an open drain MOS transistor which turns on. During lines 1-99 this transistor is off and resistor R22 pulls the $\overline{EOF}$ output to +15 volts. Transistor Q1 level translates the +1 to +15 volt $\overline{EOF}$ signal to TTL levels and inverts the signal at P3, pin 8 (EOF).

$\overline{ØX1}$ and $\overline{ØX2}$ are the X BBD clock, $\overline{ØY1}$ and $\overline{ØY2}$ the Y Dynamic Shift Register clock. $\overline{LR}$ is the Line Reset, and $\overline{LT}$ the line transfer signal. See Figure 15, "MC520 Camera Timing Diagram", for timing relationships of these signals.

Operational Amplifier U5 forms a virtual ground at inverting input pin 2. Resistors R32 and R34, and potentiometer R33 add the odd and even video signals from pins 12 and 13 of the array, U4. Potentiometer R33 provides for balancing any gain differences between the odd and even video outputs.

Network R31,C20, and C21 provide "feed-forward" compensation of Op-Amp. U5, significantly increasing its bandwidth.

Op-Amp U6 is a long-time-constant integrator in a negative-feedback loop around Op-Amp U5. The video output of U5 appears to be AC coupled as a result of this feedback. The integrator time constant is such that over a maximum line integration time of 400 microseconds, the video cannot change more than 4 millivolts due to the AC coupling. Therefore, DC restoration can be accomplished in the video processing at the beginning of each line without any degradation of the video low frequency response.

The video output of Op-Amp U5 on P3 pin 3 averages around the DC level set by V_{REF} on P3 pin 2. This DC level is derived from the Driver board A3, discussed in a later paragraph of this section, and provides for equal input voltage levels to the video differential output amplifier on that board.

The output of integrator U6 is a signal proportional to the average intensity of the camera field of view. This signal is brought to P3 pin 9 where it is further processed on the control board, A2, to operate an automatic iris lens. Operation of the auto-iris lens will be discussed in the paragraph describing the A2 board.

Finally, voltages VQ1,VQ2,VBB, and VBUF are adjustable by means of potentiometers on the control board A2. VQ1 and VQ2 provide background bias ("Fat Zero") for the odd and even BBD devices. Adjustment of VBB and VBUF provides minimum "blooming" of the array with high illumination. All adjustments will be described in Section 6 "Installation and Adjustment."

7.4 CONTROL BOARD-A2

Refer to the A2-Board Functional Diagram, Figure 16, during the following discussion.

Flip-Flop, U4 A, generates the X BBD clock, complementing on receipt of each MCLK pulse from the line receiver on the A3 board. This line receiver converts the differential MCLK signal from the controller to TTL levels suitable to clock F-F U4A.

The complementing action of U4A is interrupted during receipt of the M1C pulse from the line receiver on the A3 board. Again, this receiver converts the differential M1C signal from the controller to TTL levels. The M1C pulse is synchronized to a Flip-Flop in the controller which duplicates the action of U4A so that M1C goes true when U4A pin 5 goes true, and U4A pin 6 goes false. M1C is inverted by U2D and becomes the line transfer pulse (LT) at the Array, U4, on the A1 board. M1C is also inverted twice through U2E and U2A and clocks Flip-Flop U4B on its leading edge. This complements FF U4B, whose outputs become $\emptyset$Y1 and $\emptyset$Y2 at the Array, U4, on the A1 board. This advances the array to the next sequential line which is transferred into the X Bucket Brigades by the LT pulse. During the line transfer pulse $\emptyset$X1 is held false by inverting M1C through U2E and connecting the resulting signal to "NAND" gate U5B pin 5. This forces the output of U5B, pin 6, to be true and thus $\emptyset$X1 to be false.

Flip-Flop U4A is allowed to continue complementing two more times during line transfer and then $\emptyset$X2 is forced to be true for the remainder of the line transfer interval.

This is accomplished by releasing Flip-Flop U3A from reset during the M1C pulse. The clock input of U3A is connected to the $\emptyset$X2 output of U4A, pin 5, which sets U3A when U4A, pin 5, goes true. This occurs two pixel intervals after the M1C pulse is received by the camera. When U3A sets, its output on pin 6 goes false. This output connects to the set input, pin 4, of U4A, forcing $\emptyset$X2 to be held true until the M1C pulse goes false. When M1C goes false, Flip-Flop U3A resets and Flip-Flop U4A continues to complement on each received MCLK pulse thereafter. This generates $\emptyset$X1 and $\emptyset$X2 at the Array in such a manner that the line just transferred into the BBD's is shifted out in serial fashion.

The "odd" cycling of ØX1 and ØX2 during line transfer causes a "fill and spill" cycle in the BBD's which eliminates loss of charge at low light levels, and thus increases the Array dynamic range and linearity.

Flip-Flop U4B complements each time the M1C pulse is received from the controller, and each time advances the Array to the next sequential line.

Flip-Flop U3B complements at the same time as U4B and its output pin 9 drives chopper transistor Q1. Q1 is connected between ground and a signal which is the proportionate sum of UVID, J3 pin 3, and VAVG, J3 pin 9. The sum of these signals occurs through resistors R1 and R2. The signal at Op-Amp U1 pin 3 is then an amplitude modulated square wave at a frequency of 1/2 the camera line rate, and an amplitude proportional to the sum of UVID and VAVG.

The square wave is amplified in the non-inverting amplifier U1 developing a VIRIS signal at P2 pin 11, which is subsequently connected to an automatic iris lens if this option is ordered with the camera. The square wave form of VIRIS signal is required since the auto-iris lens responds to the peak-to-peak value of the signal and is AC coupled. The sum of UVID and VAVG, with proportionality constants determined by R1 and R2, provides proper gain and damping constant for smooth operation of the auto-iris servo loop. R5, VIRIS Zero Adjust, allows zero adjustment of the modulated square wave amplitude with the photodiode array in darkness.

And, finally, R20 and R19 provide adjustment and balancing of VQ1 and VQ2, "fat zero" bias, and R21 and R23 provide adjustment of VBB and VBUF respectively. All adjustment procedures will be described in Section 6 "Installation and Adjustment."

7.5 DRIVER BOARD-A3

Refer to the A3 board Functional Diagram, Figure 17, during the following discussion.

Digital line receivers U1A and U1B receive the M1C and MCLK differential signals from the controller, and convert them to TTL levels on P2 pins 7 and 6 respectively. These signals are then passed to the Control Board-A3; see 7.4 for a description of how these signals are used on the control board.

The MCLK output on U1B pin 2 is also connected to the input of line transmitter U2B pin 2 and is transmitted back to the controller as CCLK, where it is used to synchronize the controller with the camera video. This process in effect elininates cable propagation delays between camera and controller up to a one pixel delay.

The input to line transmitter U2A connects to the EOF signal on J2 pin 9, and transmits this signal to the controller where it is used to Frame Synchronize the controller logic.

The UVID and VREF signals connect to the differential inputs of amplifier U5 pins 1 and 2 respectively. VREF is generated by voltage divider R15 and (R14 + R17) and is passed to the Array Board A1, where it forces the average DC level of UVID to be equal to VREF. The differential output of amplifier U5 appears to be AC coupled, with gain adjusted by R20, and is forced to average around zero volts by an Op-Amp feedback loop formed by resistors R23 and R24 and amplifier U6. R23 and R24 sum the two differential output levels at pins 6 and 12 of U6, and force this sum to be the level at pin 3 of U6, i.e. ground. Amplifier U6 automatically adjust the supply voltage to the differential amplifier load resistors R22 and R25 to force this condition.

The differential amplifier outputs connect to analog line drivers U7 and U8, providing a 2 volt p-p 50 ohm differential output which is AC coupled and averages around ground level. This low impedance output will drive up to 75 feet of cable between camera and controller. The digital camera signals will also drive this length of cable, with the maximum length being limited to $\left[\frac{227}{FMHz} - 16\right]$ feet, or 75 feet, whichever is less. FMHz is the pixel scan rate. For 5 MHz, maximum length would be $\left[\frac{227}{5} - 16\right]$ = 29.4 feet (8.96 m). The 75 foot limit is set by DC voltage drops in the cable reducing the power supply voltages from the controller below the minimum requirements of the camera.

All camera I/O signals so far described enter and exit the camera through Bendix connector J4 on the camera rear panel. In addition, three BNC connectors mounted just below J4 carry Line Sync (Left BNC), Frame Sync (Right BNC) and Video (Center BNC).

The Line Sync is the M1C signal, previously described, buffered by a TTL inverter and connected to the BNC through a 50 ohm resistor. The Frame Sync is the EOF signal buffered by a TTL inverter and connected to the BNC through a 50 ohm resistor. The video BNC connects to one side of the differential video output through a 50 ohm resistor. The BNC outputs are intended as test points only, and should be loaded with no less than 1K Ω during testing. During normal operation the video BNC should be unloaded, as this would unbalance the differential signal to the controller. The Sync BNC's can be loaded during normal operation without affecting camera performance.

SECTION VIII

PRINCIPLES OF OPERATION
RS520 CONTROLLER

8.1 INTRODUCTION

This section contains an overall functional description of the RS520 controller electronics which are contained on three printed circuit cards within the controller housing. See Figure 5 for P/C card location, Figure 6 for a simplified electronics diagram, and Figure 19 for a logic flow diagram.

The P/C cards are designated A4, A6, and Interconnect, and their operation will be described in conjunction with the MC520 camera.

8.2 MC520 CAMERA

The MC520 camera connects to the CAMERA connector on the controller rear panel. The controller provides power and synchronizing signals to the camera, and in return receives video and synchronizing signals from the camera. A connecting cable up to 75 feet long may be used between the camera and controller, depending on the camera scan rate. The maximum length can be determined from the formula:

$$\text{Length} = \left[\frac{227}{\text{FMHz}} - 16\right] \text{ feet}$$

or 75 feet, whichever is less. FMHz is the maximum scan rate used. For 5 MHz, the maximum length would be $\left[\frac{227}{5} - 16\right]$ feet = 29.40 feet (8.96 m).

8.3 DIGITAL BOARD - A4

Refer to the A4 Board Functional Diagram, Figure 20, during the following discussion.

8.3.1 "M" Register

Flip-Flops U7A and U7B are connected to form a three stage ring counter. The three states of this counter are, (Ø) U7A and U7B reset, (1) U7A set, (2) U7B set. The ring counter is called the "M" register, and the three logically true output signals are MØ, M1, and M2.

The register is advanced from M1 to M2 to MØ states by clock pulses on pins 3 and 11 of U7A and U7B respectively, and from MØ to M1 states by directly setting U7A on pin 4. The clock pulses are derived from two sources and "OR" gated by U5B and U3A. Source one is the terminal count output of the pixel counter U8 and U9 on pin 15 of U9 (PTC), and source two the terminal count output of the retrace counter U11 on pin 15 (RTC). The pixel counter is enabled only when M2 is true, the retrace counter only when M1 is true; therefore, when MØ is true the register can be advanced to M1 only by directly setting M1 on U7A pin 4. This direct set is provided by the start logic to be described in the next paragraph.

The MØ state is, then, the camera start/stop state, the M1 state is the retrace state during which the next line is transferred to the Array BBD's, and the M2 state is the data output state during which each pixel value is serially output from the controller as each is counted to assure that only 100 are output per line.

8.3.2 Start Logic

When the "M" register is in the "MØ" state, a new line scan will not commence unless the register is advanced to the "M1" state by a set signal on U7A pin 4. The logic must automatically generate this advance after each line, except after line 100 where the advance to line 1 must be automatic if internal start is selected, or under user command if external start is selected.

The advance from MØ to M1 state occurs each time Flip-Flop U4A is set, and in turn its $\overline{Q}$ output pin 6 connects to U7A pin 4 causing it to set. When U7A sets, the "M" register advances to the M1 state and Flip-Flop U4A resets since MØ connects to its reset pin 1. Flip-Flop U4A then generates narrow pulses lasting only long enough to advance the "M" register.

Flip-Flop U4A is set each time ØX2B goes true on its clock pin 3 and its D input pin 2 is true. ØX2B goes true at the beginning of each even pixel, but Flip-Flop U4A cannot respond except when the "M" register is in the MØ state. The controller timing diagram, Figure 9, shows this can only occur at the end of the last pixel (D1) of each line, thus initiating a new line at the correct time if the D input of U4A is true.

The D input of U4A pin 2 will be true if the output of "NAND" gate U6A pin 3 is true. This will occur if either of its two inputs on pins 1 or 2 is false.

Pin 2 is false if (MØ • EOF) is false; therefore, a new line scan will be automatically generated for lines 1-99 since EOF is false during lines

1-99. However, during line 100, and when the "M" register is in the MØ state, pin 2 of U6A goes true. A new line scan will not be generated unless pin 1 of U6A is false. The controller cannot begin a new frame (line 1) until this condition occurs.

Pin 1 of "NAND" gate U6A connects to the $\overline{Q}$ output of Flip-Flop U4B which will go false whenever U4B is set, thus initiating a new frame scan. U4B can be set only during the MØ and M1 states of the "M" register since $\overline{M2}$ is connected to U4B reset pin 13, and the earliest U4B can be set is one pixel interval after MØ, which is also one pixel interval before the end of a line. This allows U4B to be set one pixel interval before U4A requires it to initiate a new frame, thus eliminating any race problems.

Therefore, at the end of each frame, if U4B is set, the controller will immediately begin a new frame with line 1. If U4B is not set, the controller will stop scanning until U4B is set. U4B can be set in two ways, depending on the setting of switch S1-C3. If the switch is set in the Internal Start mode, resistor R4 will cause the D input, pin 12, of U4B to be continuously true, and the controller will automatically and continuously generate new frame scans. If switch S1-C3 is set in the External Start mode, line receiver U1A is connected to the D input of U4B, and initiation of new frames is under control of the user input signal ESTART. If ESTART is held continuously true, the controller will continuously generate frames. If ESTART is false at the end of a frame, the controller will stop scanning until it is true and ØX1B goes true.

Note: Data contained in lines 1 and 100 of each frame is invalid when the system is operated in external start mode.

8.3.3 Retrace Counter

The Retrace Counter, U11, is enabled when the "M" register advances from the MØ to the M1 state by the M1 signal on pin 9. The counter counts the master clock pulses (MCLK) on pin 2, and produces a terminal count pulse on pin 15 after a number of pulses determined by the setting of S2 has been counted. Although the count may be set from 1 to 15, two counts are required for the camera "fill and spill" cycle. To these two counts additional counts are required to make the total time in the M1 state at least 2 microseconds. This is the minimum time required to transfer a line into the Array BBD's. The minimum count is then found from the equation:

$$\text{Count Min.} = 2(\text{FMHz} + 1)$$

where FMHz is the maximum pixel rate. For 5MHz operation the minimum count would be 2(5+1) = 12, and this count would provide proper operation over the entire frequency range of 0.25-5MHz; however, at frequencies below 5MHz,

the retrace time would be greater than necessary. For minimum time use the formula above and the actual pixel rate used.

When counter U11 reaches the selected count the RTC pulse is generated on pin 15, which advances the "M" register to the M2 state by clocking the register through "NOR" gate U5B and inverter U3A.

8.3.4 Pixel Counter

The Pixel Counter, formed by cascading devices U8 and U9, is enabled when the "M" register advances from the M1 to M2 state. The counter counts the ØX2B clock on pin 2, which occurs every other pixel. The counter then produces a terminal count pulse on pin 15 (PTC) after 50 ØX2B cycles or 100 pixels in a video line.

The PTC pulse advances the "M" register from the M2 state to the MØ state by clocking the register through "NOR" gate U5B and inverter U3A, completing a "M" register cycle.

8.3.5 Master Clock Generator

The Master Clock Generator is formed by one-shot multivibrators U12A and U12B connected such that they are self-triggering, producing a continuous series of output pulses whose width is determined by R21 and C3, and frequency by R18 and C1. The resulting MCLK signal is used to synchronize and determine the pixel scanning rate of the camera/controller system.

If External Clock is selected by S1-C4, one-shot MV U12A is disconnected, and line receiver U1B is connected to the trigger input pin 12 of U12B. An External Clock Signal (ECLK) from the user will then trigger One-Shot U12B generating Master Clock signals synchronized to the user clock. NOTE: If S1-C4 is switched to External Clock and then back to Internal Clock, Controller AC Power must be turned off and on to start the clock generator.

Clock Frequency, either internal or external, may be set to any value between 0.25 and 5MHz, and Clock Pulse Width may be set between 100 nanoseconds minimum to 300 nanoseconds maximum, but should not be more than 60% of the clock period. The MCLK signal is transmitted to the MC520 camera by line transmitter U13B.

8.3.6 Camera Clock Duplicator

Flip-Flops U10A and U10B duplicate the action of the camera pixel clock generator (ØX1 and ØX2), except for the "fill and spill" cycle. The U10A Flip-Flop complements on each MCLK pulse, and U10B on each CCLK pulse. Complementing is stopped and the ØX2 outputs are held true during the line retrace interval by the M1 signal connected to the set pin 4 of U10A through "NOR" gate U5A and inverter U35, and the $\overline{\text{M1D}}$ signal connected to set pin 10 of U10B.

The PTC signal on pin 3 of U5A prevents a lockup condition between the pixel counter and ØX2B that it counts.

The resulting ØX2B and ØX2D clocks are used in the controller for counting and synchronizing as described in other paragraphs of this section.

8.3.7 Logic Deskew Register

The (MØ · EOF), M1, and M2 signals must be re-synchronized to the MCLK to remove unwanted time skew between them produced by logic propagation delays.

This is accomplished by the Logic Deskew Register formed by Flip-Flops U14A, U14B, U15A and U15B.

The signals to be synchronized are connected to the D inputs of Flip-Flops U15A, U14B, and U15B respectively. The MCLK signal on the C input of each Flip-Flop strobes the D inputs, producing the (MØ · EOF) RS, M1RS, and M2RS signals on the Flip-Flop Q outputs. These signals are identical to the input signals, but delayed by one clock period, and edge synchronized to the MCLK strobe.

Flip-Flop U14A further delays the M1RS signal connected to its D input pin 2. This is done by strobing the M1RS signal with the $\overline{\text{MCLK}}$ signal on the C input pin 3. The delay is then equal to the MCLK pulse width. The delayed signal M1RSD connects to line transmitter U13A which generates the M1C signal to the MC520 camera. The delay provided by U14A eliminates any race conditions that might exist between the M1C and ØX1 and ØX2 signals in the camera.

The purpose of the logic deskew register is, then, to eliminate logic propagation delays which might cause race conditions in the following logic.

8.3.8 Cable Deskew Register

The interconnecting cable between the MC520 camera and RS520 controller generates a 4 nanosecond per foot round-trip propagation delay. In order that the controller logic remain synchronized with the camera video, a clock signal (CCLK) is transmitted from the camera to the controller where it is received by line receiver U2B, inverted by U3E and U3F, and used to strobe the cable de-skew register U17A, U17B, and U18A on their C inputs. The resulting outputs, (MØ · EOF)D, M1D, and M2D on the Flip-Flop Q outputs are the previous logic de-skewed signals now synchronized to the camera clock (CCLK). The Cable Deskew Register can correct for cable and logic delays which total one pixel interval. Therefore, cable length must be adjusted to a maximum length defined by the following formula.

Max. Length = $\left[\frac{227}{FMHz} - 16\right]$ feet, or 75 feet, whichever is less. FMHz is the maximum pixel rate to be used. For 5MHz operation, the maximum cable length must be $\left[\frac{227}{5} - 16\right]$ = 29.4 feet (8.96 m). The 75 foot length is determined by voltage drops in the interconnecting cable which reduce the camera operating voltages below normal.

The Cable Deskew Register, then, re-synchronizes the MC520 camera and RS520 controller, eliminating race problems due to interconnecting cable propagation delays.

8.3.9 Enable and Re-Reference Registers

The final synchronizing signals from the controller to the video processing P/C board and the user I/O connectors are generated by Flip-Flops U16A, U16B, and U18B, and by gating these Flip-Flop output signals with $\overline{CCLKD}$ to produce the GCLK signal to be described in 8.3.10.

Flip-Flop U16A generates the Line Enable Signal which goes true at the beginning of pixel 1, and false at the end of pixel 100 of each video line.

The LEN output pin 5 of U16A goes true when ØX2D on its C input pin 3 goes true and M2D is true on its D input pin 2. Examining the controller timing diagram, Figure 9, shows these conditions occur at the beginning of pixel 2 from the camera. Therefore, LEN goes true at the beginning of pixel 2. However, the video processing on P/C board A6 delays video output by one pixel interval by the sample-and-hold electronics, so during pixel 2, from the camera, pixel 1 data is presented to the user. The LEN signal goes true, then, at the beginning of pixel 1 at the controller output.

This one pixel delay also requires an extra pixel interval at the end of a line to read out pixel 100. This interval is labeled D1 on the timing diagram, and the LEN signal should go false at the end of D1. U16A pin 5 will go false when the M2D signal on its D input is false and ØX2D on its C input goes true. The timing diagram shows that M2D goes false at the end of pixel 99 from the camera, but ØX2D does not go true until the end of pixel D1. But, as previously described, the end of pixel D1 is actually the end of pixel 100 due to the one pixel delay in the video processing; therefore, LEN goes false at the end of pixel 100 as required.

The LEN signal on U16A pin 5 connects to line transmitter U21B which makes the signal available to the user on the Data B connector.

Flip-Flop U16B generates the Frame Enable signal which goes true at the beginning of pixel 1 of line 1, and false at the end of pixel 100 of line 100.

The FEN output pin 9 of U16B goes true when ØX2D on its C input pin 11 goes true and $\overline{(M\emptyset \bullet EOF)}$D is true [(MØ • EOF)D False] on its D input pin 12. Examining the Timing Diagram, Figure 9, shows these conditions occur at the beginning of pixel 2 of line 1 from the camera. The sample-and-hold delay in the video processing causes pixel 1 data to be output while pixel 2 is being sampled, so the FEN signal goes true at the beginning of pixel 1 of line 1 from the controller.

U16B output pin 9 will go false when the $\overline{(M\emptyset \bullet EOF)}$D signal on its D input is false [(MØ • EOF)D True)] and ØX2D on its C input goes true. Again, the Timing Diagram shows that the signal (MØ • EOF)D goes false at the end of pixel 99 of line 100 from the camera, but ØX2D does not go true until the end of pixel D1 of line 100. The FEN signal will go false at the end of pixel 100 of line 100 as a result of the one pixel delay in the video processing.

Flip-Flop U18B generates the Re-Reference signal, which is identical to the M1D signal, except that when camera scanning is stopped M1D is false and Re-Reference is true during the stop interval. The Re-Reference signal is used to command DC restoration circuits in the video processing electronics on P/C board A6, and pin 8 of U18B is connected to line transmitter U20A, making the signal available to the user on the Data B connector. The signal may be used to DC restore the controller video output signal at the far end of the transmission cable, and thus eliminate any video baseline drift due to cable characteristic changes.

To fulfill the requirements, Flip-Flop U18B output pin 8 must go true at the end of each video line, and remain true until the following M1 signal goes false.

U18B pin 8 will go true whenever $\overline{M2D}$ on its set pin 10 is true (M2D false) and ØX2D on its C pin 11 goes true. $\overline{M2D}$ goes true at the end of pixel 99 from the camera during each video line. But ØX2D does not go true until the end of pixel D1 from the camera, which is the end of pixel 100 at the controller output. U18B pin 8 will remain true until $\overline{M2D}$ on set pin 10 goes false (M2D goes true), which will occur when M1 goes false, fulfilling the previously stated requirements.

8.3.10 GCLK and HCLK Generators

In some applications it is required that a clock be generated only for each pixel, and disabled during retrace intervals. In this case only 10,000 clock pulses are generated per frame. In addition, certain Reticon Measurement systems require that clock be disabled during each retrace interval except that between line 100 and line 1. These requirements are implemented in the GCLK output, and switches C1 and C2 select the mode. See Table I to determine switch settings for these options.

The GCLK signal is derived by gating the $\overline{CCLKD}$ clock from the camera with FEN and LEN signals through "NAND" gates U6D and U22A. When

C1 is open the $\overline{GCLK}$ signal at U6D pin 11 will be continuous. When C1 is closed and C2 is open, $\overline{GCLK}$ pulses will be gated by the LEN signal appearing at pin 13 of U6D. (U22A just inverts the $\overline{LEN}$ signal from pin 6 of Flip-Flop U16A.) Since LEN is false during retrace intervals no $\overline{GCLK}$ pulses will be generated.

When C1 and C2 are closed, $\overline{GCLK}$ pulses will be disabled during retrace intervals except the interval between video lines 100 and 1, where the FEN signal connected to U22A pin 1 will enable the $\overline{GCLK}$ pulses during the end of frame retrace interval.

The $\overline{GCLK}$ leading edges occur when the Binary Video (Data) output is stable, and the trailing edges when the processed (analog) video is stable. The GCLK is made available to the user through line transmitter U19B whose output is in the Data A connector.

The HCLK signal is a continuous stream of pulses derived from the Camera Clock (CCLK) and is made available to the user through line transmitter U21A whose output is in the Data B connector.

8.4 ANALOG BOARD - A6

The Analog Board - A6 will be discussed as subcircuits. Refer to the Functional Diagrams referenced in each subcircuit.

8.4.1 Video Line Receiver

In the following discussion, refer to the Video Line Receiver Functional Diagram, Figure 10, and LM1496N schematic diagram, Figure 21.

The Video Line Receiver receives video from the MC520 camera via the interconnecting cable which may be up to 75 feet long. The line receiver is designed to reproduce the video signal while eliminating to a great extent any noise signals picked up by the cable.

R6 is the cable terminating resistor, while R7,R8,R10,R11, R12 and C3 and C4 form a bridge network which can be balanced for common mode signals by means of R11 and C3. The bridge output connects to the differential inputs of amplifier U5 which subtract common mode signals and sum differential video signals.

Amplifier U5 has differential outputs on pins 6 and 12 which are converted to a single ended output by transistor Q1 and load resistors R21, R22, and R24.

Transistor Q1 further subtracts common mode signals and sums video signals. C12 provides additional fine balancing of high frequency common mode noise.

Q2 is an emitter follower which provides low impedance video output for charging capacitors in the sample-and-hold circuits to be described in the following paragraph. Gain adjustment of the Line Receiver is provided by R33.

U4 and C8 form a long-time-constant integrator which is in a negative feedback loop that forces the video output at TP1 to a average around the voltage set by voltage divider R15 and R16. This voltage is nominally +3 volts.

The video output at TP-1 then appears to be AC coupled with a time constant set by R20 and C8. This time constant is such that the average video level cannot change more than 4 millivolts over the maximum line integration time of 400 microseconds; therefore, DC restoration at the end of each line will effectively restore the video baseline. RC networks connected to pins 5,8 and 10 of U5 provide proper bias voltages for the amplifier.

8.4.2 Sample-and-Hold

In the following discussion refer to the Sample-And-Hold Functional Diagram, Figure 22.

The Sample-And-Hold circuit separates the Odd and Even pixel information, storing it on separate hold capacitors, and then multiplexes the signals to again form a single output stream of sample-and-hold video, but with improved signal to noise ratio and reduced inter-pixel switching transients. The circuit operates as follows:

Video from the Video Line Receiver connects to the source of MOS analog switches Q3 and Q4. These switches are turned on alternately by pulses from one-shot multivibrators U2A and U2B which are triggered alternately as Flip-Flop U1A complements on each CCLKD pulse on its C input pin 3. The pulses are applied to the Q3 and Q4 gates through "NAND" gates U3A and U3B which also convert the TTL level pulses to MOS levels. The $\overline{\text{RE-REF}}$ signal on pin 2 of U3A and U3B turns on both Q3 and Q4 during the line retrace interval to provide a through path to the DC restoration circuits which are operating during that time.

As Q3 and Q4 alternately close, the video levels of the Odd and Even pixels respectively are stored on capacitors C18 and C20. These levels are then connected to the gates of source followers Q9 and Q10 through capacitors C17 and C20. During a line of video information, C17 and C20 act as voltage sources rather than capacitors since the high input resistance of Q3 and Q4 prevents them from discharging. The voltages across these capacitors are in series with the video level and subtract from it. Level translation can be implemented by using this feature as follows:

The average level of the video at capacitors C18 and C20 is +3 volts determined by the output of the Video Line Receiver. The required average level at the input pins 1 and 4 of multiplex switch U8 is nominally -5 volts.

If, during the line retrace interval, an 8 volt signal is impressed across capacitors C17 and C19 it will subtract from the video signal during the following line providing the required -5 volt average input to U8. In practice the voltage impressed across C17 and C19 is made to be a value which forces the DC level at pins 2 and 3 of the multiplex switch to be equal to the DC level set by voltage divider R15 and R16 at pin 3 of op amps U6 and U7. Amps. U6 and U7 become part of negative feedback loops when MOS switches Q5,Q6, Q7, and Q8 are turned on during the Re-Reference (Retrace) interval. Switches Q7 and Q8 connect the inverting inputs of amplifiers U6 and U7 through resistors R40 and R41 to multiplex switch pins 3 and 2 respectively. The outputs of amplifiers U6 and U7 are connected through switches Q5 and Q6 to the gates of source followers Q9 and Q10 which are in turn connected to pins 1 and 4 of U8, completing the feedback loops.

Forcing the voltages at pins 2 and 3 of U8 to be equal causes the value of the current sources in device U8 to be determined by R43 and R44 for the Odd pixels and R50 and R52 for the Even pixels. The parallel value of these resistor pairs also determines the gain of the current amplifiers as well as the absolute dark level current. Two adjustments are provided which interact and must be set in a "sliding" fashion. First R50 is adjusted for zero offset between the two currents with the array dark, and then R52 is adjusted for zero current offset with the Array at 80-90% of saturation level. Then these adjustments are repeated until zero offset exist for both dark and light conditions. Once these adjustments are correct, the feedback amplifiers U6 and U7 maintain the balance conditions with variations in temperature, supply voltage, and components.

At this point, then, the video from the Line Receiver has been separated into Odd and Even pixel information and stored on capacitors C18 and C20. The levels on C18 and C20 have been level translated to the inputs of multiplex switch U8 where they are converted to currents proportional to the video voltage levels. Next, the switches in device U8 must alternately switch these currents in proper sequence to a single output resistor R57 to reconstruct again the proper odd and even pixel sequence. These switches are operated from the output signals of Flip-Flop U1B which is slaved to Flip-Flop U1A in such a manner that when U1A is causing the sampling of an odd pixel, U1B has switched the output of the previously sampled even pixel to the multiplexor output, and vice versa. Therefore, at the output of U8, the video signal to noise has been improved by the sample-and-hold action, and the inter-pixel switching transients have been reduced by the high speed switching capability of the U8 device. The switch output, pin 12, is buffered by Q1 to provide a low impedance signal source to the Blanking Switch circuits following.

To complete the Sample-And-Hold electronics description, the TTL REREF signal entering the board on pin 32 is converted to MOS levels by first buffering it by "NAND" gate (inverter) U16D, level translating with transistor Q17 and providing high current, fast-switching capability through device U17B. The signal is then applied to the level translation circuits previously discussed.

8.4.3 Blanking Switch

In the following discussion, refer to the Blanking Switch Functional Diagram, Figure 23.

During the Retrace/DC Restoration interval, large transients are introduced into the video signal. The Blanking Switch removes these transients by presenting a fixed signal level to the user during the line retrace intervals.

The operation of the Blanking Switch is similar to the sample-and-hold switch previously described, it operates as follows:

The video from the sample-and-hold circuit is connected to C29 which operates as a voltage source since the voltage across it will not be discharged by the high resistance input gate of source follower Q14. Therefore, the capacitor voltage is in series with the video data and subtracts from it. Level translation from the +6 volt average level of the sample-and-hold output signal to the -5 volt average level required at input pin 1 of switch U11 is accomplished by applying an 11 volt potential across C29 during each line retrace interval. This potential remains across C29 for the entire following video line and subtracts from its level, thus providing the required translation. The charge across C29 is replenished at the beginning of each line; therefore, it is only necessary that C29 hold its charge for the maximum line interval - 400μs. In practice, the voltage impressed across C29 is made to be a value which forces the DC level at pin 2 of U11 to be equal to the DC level at pin 3 of Op Amp U10. Op Amp U10 becomes part of a negative feedback loop when MOS switches Q12 and Q13 are turned on during the Re-Reference (Retrace) interval. Forcing the voltage at pin 2 of U11 to be a fixed value also sets the dark level value of the video current source in the U11 device to a fixed value determined by R69. This current then decreases proportionally to the light intensity on the camera Array.

A second current source in the U11 device (See Figure 21), has its current value set by forcing the voltage at pin 3 to be a value equal to the voltage at pin 3 of Op Amp U9, which is adjustable by means of R61.

This current source value is then set by the voltage at U11 pin 3, and the value of R71. Although the adjustment R61 is called Dark Level Adjust, it actually sets the value of current in the current source which is connected to the Blanking Switch output during the Blanking interval. As will be seen later, the temperature compensation feedback loop causes this adjustment to change the video dark level, not the video blanking level.

At this point, the video signal modulates one current source on device U11, and the adjustment of R61 sets the value of the second.

The switches on U11 alternately connect these two current sources to U11 output pins 6 and 12. When video current is connected to pin 6, the blanking current is connected to pin 12, and vice versa. These switches are controlled by the LEN and $\overline{\text{LEN}}$ (Line Enable) signals applied to resistor network R66, 74, 75, and 76, which level translate these signals to a value which will properly operate the switches. When the LEN signal is true, video current is connected to pin 12 of U11, when LEN is false, blanking current is connected to this pin.

The currents switched to U11 pins 6 and 12 are converted to voltage levels by load resistors R177 and R179, and these voltage levels are in turn connected to the bases of emitter followers Q22A and Q22B which provide low impedance output voltages proportional to the video and blanking currents. When video level is on the emitter of Q22B, blanking level is on the emitter of Q22A. This situation is reversed during the blanking (retrace interval).

The video and blanking levels will drift with temperature; however, they will drift identically since the current generators on U11 are integrated on a common substrate, as are also transistors Q22A and Q22B. Nevertheless, the absolute values of the video and blanking levels will drift with temperature if not corrected.

The correction is performed by recognizing that if feedback is used to force the blanking level to be constant with temperature, the automatic correction voltage generated by the feedback, if subtracted from the video signal, will eliminate its drift as well. This is true since it is known that the video and blanking level signals drift identically.

The correction is implemented as follows:

The video and blanking outputs from Q22A and Q22B, on their emitters, connect to the sources of MOS switches Q21 and Q22 through resistors R79 and R80. These switches are turned on by the LENHV and $\overline{\text{LENHV}}$ signals in such a way that the current through the switches is determined by the blanking level only, i.e., when blanking level is on the Q22A emitter, Q21 is on, and when blanking level is on the Q22B emitter, Q20 is on. Therefore, the voltage at the common drain junction of Q20 and Q21 is the blanking level at all times. Op Amp U9 is in a feedback loop which forces this blanking level on U9 pin 2 to be equal to the voltage on U9 pin 3. The latter voltage is adjustable by means of R9. The output of U9 on pin 6 is a correction voltage which adjusts automatically to hold the blanking level at the set value on U9 pin 3. This correction voltage is applied through R62, R177, and R179, and when R62 is properly balanced, corrects the video and blanking levels identically. Therefore, if the blanking level drifts with temperature, automatic correction is applied to hold it at a fixed value set by R9. This same correction is applied to the video level which eliminates its drift as well. R62 is adjusted so that the correction voltage is equally applied to video and blanking levels.

The voltage output on the emitter of Q22B is then the temperature compensated, blanked, video output which connects to the Line Driver and Threshold circuits to be described in the next paragraph. Adjustments are described in Section 6.

8.4.4 Line Drivers and Threshold Detectors

In the following discussion refer to the Line Drivers and Threshold Detectors Functional Diagram, Figure 24.

The video output from the Blanking Switch is further processed to provide a 50 ohm Z output, a 50 or 75 ohm differential output, and is also applied to threshold detectors to provide binary "Data" and "Light Level" digital output signals. The circuits providing these functions operate as follows:

8.4.4.1 Line Drivers

The video level from the blanking circuit connects to the inputs of two low impedance line drivers U14 and U15 on pin 8. The output of U14 pin 4, connects to network R92 and C51 that provides series termination and high frequency compensation to drive a 50 ohm transmission line connected to P6. P6 is connected to the controller Z output BNC on the back panel, and is intended to drive the Z axis input of a video monitor.

The output of driver U15, pin 4, connects to P5 which is not presently used in the controller, and is intended to provide video to future options.

The output of U15 also connects to resistor network R146 and R147. This network divides the video signal by two, and level translates it to the -5 volt nominal level required to properly operate differential amplifier U29, pin 1. Input, pin 4, is connected to R150 which may be adjusted also to -5 volts, thus balancing the amplifier output.

The differential outputs of amplifier U29, pins 6 and 12, connect to load resistors R155 and R156, converting the differential currents from U29 to differential voltages, which in turn connect to low impedance line drivers U12 and U13, pin 8. The low impedance outputs, pin 4, drive two output connectors, P7 and P8, through appropriate RC networks to provide 50 ohm termination at P7 and 75 ohm termination at P8. The 50 ohm video signal is available in the Data B connector, and the 75 ohm video at the Twinax connector, both on the controller rear panel. Both outputs cannot be used simultaneously.

The common mode voltage of these two differential output signals is forced to be zero volts by a negative feedback loop consisting of Op Amp U31 and resistors R152 and R153. These two resistors sum the differential

output signals on U29 pins 6 and 12, and force this sum to be equal to the voltage on pin 3 of U31,i.e., zero volts. Op-Amp U31 produces a correction voltage on its output pin 6 which is applied to load resistors R155 and R156 to automatically adjust the output common mode signal. As a result, the static output signals from U12 and U13, with respect to ground, are either zero volts (± 30mv), or one output is above ground and the other below ground by an equal amount. Differential gain is adjusted by R165, and the RC networks connected to pins 5, 8, and 10 of Amplifier U29 provide correct operating voltage levels.

8.4.4.2 Threshold Detectors

The video output of low impedance driver U15, pin 4, connects to two RC networks, R133-C99, and R134-C100, which in turn connect to the non-inverting inputs of level detectors U27 and U28 pin 4. Positive feedback from the output of U27 and U28, pin 9, through RC networks R135-C101 and R143-C108 provides hysteresis for noise free level detection. The detection levels are adjustable by means of R141 for the "Data" threshold, and R137 for the "Light Level" threshold. These adjustments set the voltage at input pin 3 of the level detectors, above which the detector output switches.

If the video signal exceeds the level on pin 3 of either U27 or U28, their output pin 11 goes false and remains false until the level drops below that on pin 3. The pin 11 outputs may remain false for as short as one pixel interval, or as long as 100 intervals. The outputs are always forced true during the line retrace interval by the LEN signal on pins 8 and 13 of U27 and U28.

The outputs of level detectors U27 and U28, pin 11, are connected to the D inputs of Flip-Flops U25A and U25B respectively. The C inputs of these Flip-Flops connect to the $\overline{\text{CCLKD}}$ signal which goes true when the video signal has reached its final level. The data from the level detectors is then strobed into the Flip-Flops where it is stored until the next pixel data arrives.

The output of Flip-Flop U25B, pin 8 is the binary "Data" output, and the output of Flip-Flop U25A, pin 6, is the binary "Light Level" output. The "Data" output connects to line transmitter U30A, pin 2, and its output is made available to the user in the Data A connector.

The "Light Level" output of Flip-Flop U25A, pin 6, connects to jumper W2 which may be connected to line transmitter U30B and is made available in the Data A connector.

If both "Data" and "Light Level" outputs are connected in the above manner, the video may be processed with dual thresholds set by R137 and R141, with the binary data available in the Data A connector.

The "Light Level" binary output can be modified to operate differently than the "Data" output by means of jumpers W1, and W3 through W7.

With W1 installed (and W2 removed) the "Light Level" line transmitter U30B connects to the Q output, pin 9, of Flip-Flop U26B. This signal, then, becomes the new "Light Level" output available in the Data A connector on the controller rear panel.

The D input of U26B connects to the Q output of U26A. This output goes true whenever a pixel level exceeds the "Light Level" threshold setting, and remains true until reset at the end of the line or the end of the frame, depending on whether jumper W6 or W7 is installed. The LEN signal through jumper W6 to pin 1 of U26A resets it at the end of a line; the FEN signal through jumper W7 to U26A resets it at the end of a frame. U26A is set by the signal to its set pin 4 which is connected to the output pin 11 of the "Light Level" threshold detector U27.

To reiterate, then, Flip-Flop U26A will set whenever a pixel level exceeds the "Light Level" threshold setting, and will remain set to the end of the line or the end of frame, depending on which jumper is installed, W6 or W7.

The output of U26A pin 5 will be strobed into Flip-Flop U26B at a time depending on which jumper is installed at its C input pin 11, W3, W4, or W5. If W3 is installed (and not W4 and W5) and a pixel exceeds the "Light Level" threshold, U26B will set at the end of the line in which the pixel exceeded threshold. If W4 is installed (and not W3 and W5) and a pixel exceeds threshold, U26B will be set at the end of the frame. If W5 is installed (and not W3 and W4), and a pixel exceeds threshold, U26B will set when that pixel level is stable.

Resetting of Flip-Flop U26B depends on the choice of jumpers W6 or W7. A more detailed discussion of jumper selection and resulting modes of operation will be found in Section VI "Installation and Adjustment".

8.4.5 X and Y Sweep Circuits

In the following discussion, refer to the X and Y Sweep Functional Diagram, Figure 25.

The X and Y sweep circuits generate linear ramp signals synchronized to the Line and Frame Enable signals. Both signals connect to 50 ohm BNC connectors on the controller rear panel, and are intended to drive the X and Y inputs of a video monitor, along with the Z output previously described, to provide a raster scan display of the camera field of view.

The X and Y sweep generator circuits are identical except for the source of synchronizing signal and the RC values in the integrator circuits, so only the X sweep circuit will be described.

Operational Amplifier U21 is connected as a standard feedback integrat with C90 as the integrator capacitor, and R112 as the integrator resistor. MOS switch Q18 across C90 discharges the capacitor during the line retrace interval. If the

voltage at the junction of R111 and R112 is a fixed level, and MOS switch Q18 is turned off, the output of U21 pin 6 will be a linearly increasing (or decreasing) voltage with a slope proportional to the fixed level. The amplitude that the "ramp" will reach will depend on how long Q18 is off. Therefore, if a correction is not made, the ramp amplitude would change if the camera scan rate is changed. This would change the picture size on the video monitor, which is undesirable.

A correction can be made by realizing that the average value of a triangular wave is equal to 1/2 of its peak-to-peak value. If the average value of the triangular wave (ramp) can be forced to be a fixed value, then the peak-to-peak value will also be fixed.

This is implemented by extracting the ramp average voltage value and correcting the integrating capacitor charging current to maintain this average at a fixed level.

Op-Amp U19 is another integrator whose time constant is determined by C79-C82 and R110 and R118. The non-inverting input of this integrator is connected to the output of the X ramp generator on U21 pin 6, and the inverting input to potentiometer R120. The output of U19 pin 6 produces a voltage which determines the X ramp charging current through R111 and R112. The U19 integrator extracts the average value of the X ramp and modifies the C90 charging current to make that average value equal to the voltage at the arm of potentiometer R120. R120 will then adjust the X ramp amplitude, and once set, the amplitude will remain fixed as the camera scan rate is varied from 0.25-5MHz.

The X ramp signal is connected through low pass filter R171-C125 to the input pin 8 of line driver U23 whose output pin 4 connects through R144 to P3. R144 provides a 50 ohm output impedance, and the signals from P3 connect to the X and Y sweep BNC outputs on the controller rear panel.

X and Y amplitude adjustments are described in Section 6.

SECTION IX

FAILURE DIAGNOSTIC PROCEDURES

9.1 INTRODUCTION

The procedures described in this section should be followed when attempting to identify the cause of faulty operation. The procedures will attempt to determine which repairable assembly is at fault. The user then has the option to further determine which component or components have failed, and replace them, or contact Reticon for authorization to return the subassembly, or, at Reticon's discretion, the entire system, for repair.

Note: Authorization must be obtained from Reticon prior to returning any system or subsystem to the factory.

When any signal output is absent or incorrect, and the cause is not obvious, follow the sequence of steps in the order listed.

Refer to the P/C board and interconnect drawings, Section VI on Adjustments, and Sections VII and VIII on Principles of Operation, during the diagnostic procedures.

9.2 TEST INSTRUMENTS

The following are required for some steps in the diagnostic procedures:

1. Dual trace oscilloscope with delayed sweep
2. Digital Voltmeter
3. Potentiometer adjusting tool
4. Small flat blade screwdriver
5. Phillips #2 screwdriver
6. Allen wrench - 1/16 inch.

9.3 EXTERNAL CONNECTIONS

Before continuing diagnostics, check that all necessary signal and power cables are connected between camera and controller, controller and users equipment, controller and AC line.

If necessary, check continuity of user supplied interconnect cables using Drawing 022-0063 as a reference.

If the red power indicator on the controller front panel does not illuminate when the power switch is depressed, check the line cord connection to the AC power source, check that the indicator lamp has not burned out, and that the line fuse on the controller rear panel has not blown.

Replace the lamp and fuse with proper rating as necessary. If the fuse continues to blow, the power supply may be defective, and the entire system should be returned to Reticon for repair.

If the line fuse and indicator lamp are not defective, but the system is still inoperative, continue with the diagnostic procedures.

9.4 RS520 POWER SUPPLY

CAUTION: Although care has been taken to cover terminals connected to 115 or 220 V.A.C., caution should be used when making measurements and adjustments, and while removing P/C boards within the controller.

Remove the controller top cover by means of the two Phillips screws at its rear corners.

If the line fuse and power indicator lamp are not defective, but the lamp still does not illuminate, or the system is still inoperative, check the ± 15 volt and +5 volt outputs of the supply. The supply output terminals may be located from Figure 27.

These voltages should be within 100 millivolts of their nominal values. If not, adjust them by means of the potentiometers shown in Figure 27. If adjustment is ineffective, either the supply is faulty, or an overload condition exists.

With power off, remove the RS520 P/C board retaining cover by means of the five Phillips screws. Carefully remove the plugs, P2-4, and P6-8, on the side of the A6 board, noting how to properly reinstall them.

Carefully remove the A4 and A6 boards, noting also how to reinstall them.

Disconnect the MC520 camera cable at the controller rear panel.

Turn on power and recheck the power supply voltages. If the voltages still cannot be adjusted, either the power supply or the controller interconnect board is faulty. It is best that the controller be returned to Reticon for repair of either of these problems.

If, however, the voltages return to normal, the overload is in the MC520 camera or on the A4 or A6 P/C boards.

Isolate the overload source by installing the A4 board, A6 board, and camera, one at a time, while observing which one causes the overload condition.

If a board is at fault, repair it, if the MC520 camera is at fault, go to 9.16.

With power restored, check overall system operation, and continue diagnostics if necessary.

9.5 RS520 MASTER CLOCK GENERATOR

If the controller Master Clock Generator is malfunctioning, all other system output signals, analog and digital, will be affected. To determine if a malfunction exists, check the following signal with an oscilloscope. Refer to Drawings 010-0224, 011-0224, and 005-0082.

1. Check for 5 volt, positive, 100 nanosecond (Adjustable) wide pulses at TP-1 (MCLK) on the RS520 A4 board. Pulse frequency can be adjusted by R18 & C3, pulse width by R21. Adjust the pulse width if necessary. (See Section VI.)

   If pulses are not present, assure that the proper clocking mode has been selected, i.e., either internal or external (See Table I). If external is selected, make sure the clock pulses from the users equipment are present at pin 12 of device U12B on the A4 P/C board. If internal clock is selected, and pulses are still not present at TP-1, repair the A4 board.

   Note: If the internal/external clock selector switch, S1-C4, is set for external, and then returned to internal, the RS520 power switch must be turned off and then on to restore the MCLK signal.

With MCLK pulses restored, check the entire system for proper operation. If other signals are incorrect, proceed with the diagnostic steps.

9.6 RS520 "M" REGISTER

If the "M" register is malfunctioning, all other system output signals, analog and digital, will be affected. To determine if a malfunction exists, check the following signals with an oscilloscope. Refer to Drawings 010-0224, 011-0224, and 005-0082.

1. Check for 5 volt, positive pulses at TP-2 (M1) on the RS520 A4 board. The width of these pulses is determined by the setting of Retrace Count Switch-S2. Set this switch group as described in Table II. If M1 pulses are not present, assure that the proper starting mode has been selected, either internal or external as required. (See Table I.) If external has been selected, check that external start pulses from the users equipment are present at pin 12 of device U4B on the A4 board. If internal start is selected, but M1 pulses are still not present at TP-2, repair the A4 board.

2. If the M1 signal is present at TP-2, but is not properly synchronized as shown in the RS520 & MC520 Timing Diagrams, Figures 9 and 15, check that EOF pulses from the camera are at pin 3 of device U2A on the A4 board. If these EOF pulses are not present, go to 9.17. If they are present, repair the A4 board to correct the synchronization problem.

   With M1 pulses restored, check for proper overall system operation. If signals are still incorrect, proceed with the diagnostic tests.

9.7 RS520 LOGIC DESKEW REGISTER

If the Logic Deskew Register is malfunctioning, all other system output signals, analog and digital, will be affected. To determine if a malfunction exists, check the following signals with an oscilloscope on the RS520 A4 board. Refer to Drawings 010-0224, 011-0224, 005-0082.

1. Connect one trace of the oscilloscope to pin 2, and the second trace to pin 5 of device U15A. Check that the pin 5 signal is identical to the pin 2 signal, except delayed by one clock (MCLK) period.

2. Check pins 12 and 9 of device U14B as in item 1 above.

3. Check pins 2 and 5 of device U15A as in item 1 above.

4. Check pins 2 and 5 of device U14A as in item 1 above, except delay should be on clock period plus one clock pulse width.

If the above signals are absent or incorrect, repair the A4 board.

With the Logic Deskew Register operating properly, check overall system operation. If signals are still incorrect, proceed with the next diagnostic step.

9.8 RS520 CABLE DESKEW REGISTER

If the Cable Deskew Register is malfunctioning, all other system output signals, analog and digital, will be affected. To determine if a malfunction exists, check the following signals with an oscilloscope on the A4 board. Refer to Drawings 010-0224, 011-0224, 005-0082.

1. Connect one trace of the oscilloscope to pin 2, and the second trace to pin 5 of device U17A. Check that the pin 5 signal is identical to the pin 2 signal, except delayed by the camera connecting cable propagation delay of approximately 4 nanoseconds per foot.

2. Check pins 2 and 5 of device U18A as in item 1 above.

3. Check pins 12 and 9 of device U17B as in item 1 above.

If all these signals are absent, check that CCLK pulses are arriving from the camera on pin 2 of device U2B on the A4 board. If pulses are not present, go to 9.17.

If these CCLK pulses are present, but not all of the Logic Deskew Register signals are correct, repair the A4 board.

With Logic Deskew Register signals correct, check for proper overall system operation. If any signals are still incorrect, continue with the following diagnostic checks.

9.9 RS520 ENABLE AND RE-REFERENCE REGISTERS

If the Enable and Re-Reference Registers are malfunctioning, all other system output signals, analog and digital, may be affected. To determine if a malfunction exists, check the following signals with an oscilloscope on the RS520 Data A and Data B connectors. Refer to Drawings 010-0224, 011-0224, and 022-0063.

1. Check pins N and P on the Data A connector (J10) on the RS520 rear panel for 5 volt positive and negative pulses respectively. The positive pulse (FEN+) should go true at the beginning of pixel 1 of line 1, and false at the end of pixel 100 of line 100. Check that the FEN signal is also at the Sync BNC also on the RS520 rear panel.

   If any signals are incorrect, repair the A4 board, check system operation, and continue diagnostics if necessary.

2. Check pins B and C on the Data B connector (J11) for 5 volt positive and negative pulses respectively. The positive pulse (LEN+) should go true at the beginning of pixel 1 and false at the end of pixel 100 of each video line. The oscilloscope may be synchronized from the Sync BNC jack for this test. If the LEN signal is incorrect, repair the A4 board, check overall system operation, and continue diagnostics if necessary.

3. Check pins K and L of the Data B connector (J11) for 5 volt positive and negative pulses respectively. The positive pulse (REREF+) should go true at the end of each video line, and false two clock periods (MCLK) before pixel 1 of the next video line. If the camera scan is stopped, the REREF signal should remain true until two clock periods before pixel 1 of line 1. The oscilloscope may be synchronized from the Sync BNC jack for this test. If the REREF signal is incorrect, repair the A4 board, check overall system operation, and continue diagnostics if necessary.

9.10 RS520 GCLK, HCLK, AND MØ•EOF LOGIC

The GCLK output signal appears on the Data A I/O connector, and the HCLK and (MØ•EOF) signals on the Data B connector. If these signals are incorrect, operation of the users equipment utilizing these signals will be affected. To determine if a malfunction exists, check the following signals with an oscilloscope. Refer to Drawings 010-0224, 011-0224, and 022-0068.

1. Check pins M and N on the Data A connector (J10) for 5 volt positive and negative pulses respectively. The positive pulse (GCLK+) true interval varies with clock frequency, and the false interval is adjusted by the clock pulse width. See Section VI for adjustment procedures. If these pulses are present, set switches S1-C1 and S1-C2 per Table II, items 1, 2, and 3. After each setting, check that the GCLK+ pulses are as described in the table. The oscilloscope may be synchronized from the Sync BNC jack for these tests.

If the GCLK pulses are incorrect, repair the A4 board.

2. Check pins M and N of the Data B connector (J11) for 5 volt positive and negative , 100 nanoseconds wide, pulses respectively. The positive pulse (HCLK+) true interval varies with the MCLK pulse width, and its frequency with MCLK frequency. See Section VI for adjustment procedure, and adjust as necessary.

   The HCLK should be a continuous train of pulses, if they are incorrect, repair the A4 board.

3. Check pins P and U of the Data B connector (J11) for 5 volt positive and negative pulses respectively. The positive pulses (MØ•EOF) should agree with the RS520 timing diagram, Figure 9, at A4U5C-10.

   Note: On RS520 controllers with serial numbers 78083 through 78091 the M2 signal appears on pins P and U of J11. This signal should agree with the timing diagram, Figure 9, at A4U7B-9. See Section VI for instructions to change the M2 signal to the MØ•EOF signal if required.

   If the MØ•EOF or M2 signal is incorrect, repair the A4 board, and then check overall system operation. If other signals are incorrect, continue diagnostics.

9.11 RS520 ANALOG LINE RECEIVER

If the Analog Line Receiver is malfunctioning, all video and binary data outputs will be affected. To determine if a malfunction exists, check the following signals with an oscilloscope. Refer to Drawings 010-0225, 011-0225, 005-0082, and 022-0063.

1. Remove P2 on the RS520 A6 P/C board and, with the MC520 camera in darkness, check that pins 1 and 3 of P2 are within ± 100 millivolts of ground. If correct, check the same pins on P2 for a 2 volt p-p video signal with the camera at light saturation. If either signal is incorrect, go to 9.18. If both DC level and video are correct, reconnect P2 and continue with diagnostics.

2. With the camera in darkness, check at TP-1 on the A6 board for a DC level of +3 volts nominal. If this voltage is correct, check for a 2 volt p-p video signal with camera in light saturation. If the DC level is incorrect or the video absent, repair the A6 board. If the video level is present, but not 2 volts p-p, see Section VI for adjustment procedures.

With the Video Receiver operating properly, check overall system operation, and continue diagnostics if necessary.

9.12 RS520 SAMPLE AND HOLD

If the Sample-and-Hold circuits are malfunctioning, all Video and Binary Data outputs from the controller will be affected. To determine if a malfunction exists, check the following signals with an oscilloscope. Refer to Drawings 010-0225, 011-0225, and 005-0082.

1. With the MC520 camera in darkness, check TP-2 on the A6 board for a nominal +6 Volt DC level. If the DC level is correct, check that 2 volt p-p negative video appears at this test point with the camera in light saturation. If the DC level and video are correct, but the pixels have gain or offset unbalance, see Section VI for adjustment procedure.

   If the DC level and video are incorrect, repair the A6 board. If only the video is incorrect, check TP-6 and 7 on the A6 board for 5 volt, positive, 150 nanosecond wide pulses. If pulses <u>are</u> present, but not correct width, see Section VI for adjustment procedures.

   If the 150 nanosecond pulses <u>are not</u> present, repair the A6 board.

With the Sample-and-Hold circuits functioning properly, check overall system operation, and continue diagnostics if necessary.

9.13 RS520 BLANKING SWITCH AND LINE DRIVERS

If the Blanking Switch is malfunctioning, all Video and Binary Data outputs from the controller will be affected. To determine if a malfunction exists, check the following signals with an oscilloscope. Refer to Drawings 010-0225, 011-0225, 022-0051, and 005-0082

1. With the MC520 camera in darkness, synchronize the oscilloscope on the Sync BNC connector and check the Z BNC connector for a blanking level and dark level that can be adjusted from +0.2 to -2 volts with the Z connector unterminated. See Section VI for adjustment procedure.

2. Check TP-5 on the A6 board for signals as in item 1 above.

3. Check the Video 75(+) and 75(-) outputs on the 75 ohm Twinax connector for signals as in item 1 above. The 75(-) signal should be the complement of the 75(+) signal. If the 75 ohm output transmitter requires gain adjustment, see Section VI.

If any of the above signals are incorrect, or cannot be adjusted properly, repair the A6 board.

With the Blanking Switch and Line Drivers functioning properly, check overall system operation, and continue diagnostics if necessary.

9.14 RS520 THRESHOLD DETECTORS

If the Threshold Detectors are malfunctioning, the Binary Data and Light Level outputs to the users equipment will be incorrect. To determine if a malfunction exists, check the following signals with an oscilloscope. Refer to Drawings 010-0225, 011-0225, 022-0063, and 005-0082.

1. With the MC520 camera at approximately 50% light saturation, and with the oscilloscope traces on pins H and G of the Data A connector (J10), adjust the Data Threshold potentiometer above and below the 50% level, observing that pin H goes true when the adjustment is below the 50% point and false when above. The signal on pin G should be the complement of that on pin H.

2. Check pins L and K on the Data A connector (J10) as in item 1 above, but adjust the Light Level Threshold potentiometer above and below the 50% level. These outputs will respond in various ways, depending on jumper options on the A6 board. See Section VI to determine what response should occur.

If either of the above signals is incorrect, check that the proper jumper options are installed (Section VI), and repair the A6 board if necessary.

With the Threshold Detectors operating properly, check overall system operation, and continue diagnostics if necessary.

9.15 RS520 X and Y SWEEP

If the X and/or Y sweep circuits are malfunctioning, the monitor raster will be incorrectly formed. To determine if a malfunction exists, check the following signals with an oscilloscope.

1. Check for a linear sweep (ramp) at the X BNC jack on the RS520 rear panel. The ramp should begin at pixel 1 of each video line and end at pixel 100. The X Amplitude Adjustment should vary the signal amplitude from +2 to -2 volts p-p with the X output unterminated.

2. Check as above on the Y BNC jack, except that the ramp should begin at pixel 1 of line 1 and end at pixel 100 of line 100.

If either of the above signals is incorrect, repair the A6 board.

9.16 CAMERA POWER OVERLOAD

If it is determined that a power overload condition exists in the MC520 camera, the camera must be opened and each of the three individual P/C boards disconnected until the overload is isolated to a particular board. Before opening the camera, remove the Bendix connector (P4) on the rear panel, and check that the controller supply voltages return to normal. This assures that the overload condition is due to the camera.

When this has been determined, open the MC520 camera as follows: (Refer to Figure 2)

1. With all cables disconnected from the camera, remove the six Allen Head screws around the edge of the camera rear panel.

2. Carefully remove the rear panel. It may be necessary to reconnect the Bendix connector and use it as a "handle" to break the gasket seal. Pull the rear panel away from the camera until the flexible cable connecting the A1 and A2 boards is almost fully extended. Unplug the flexible cable from the A2 board, noting how to reconnect it.

4. Reconnect the camera to the controller (P4), and check the controller supply for the overload condition. If the overload no longer exists, repair the MC520 A1 P/C board.

5. If the overload still exists, remove P4 and the two Phillips head screws holding the A2 board to the A3 board. Carefully unplug the A2 board, noting how to reinstall it.

6. Again reconnect P4 and check for the overload condition. If it still exists, repair the A3 board. If it does not exist, repair the A2 board.

With the overload condition corrected, check overall system operation, and continue diagnostics if necessary.

9.17 MC520 MCLK, CCLK, M1, AND EOF LOGIC

If the RS520 controller is not receiving CCLK or EOF signals from the camera, check the following with an oscilloscope. Refer to Drawings 010-0222, 011-0222, 010-0242, 011-0242, 010-0223, 011-0223, 022-0051.

1. Check the following signals at connector P1 on the camera A3 P/C board. Small openings in the side of the plug block make these signals available.

   (a) On pins 16 and 17, 5 volt, positive and negative, 100 nanosecond wide pulses (MCLK) from the controller.

   (b) On pins 21 and 22, 5 volt, positive and negative, 100 nanosecond wide pulses (CCLK) from the camera.

If the MCLK pulses are absent, repair the connecting cable or controller A4 P/C board.

If the CCLK pulses are absent, repair the camera A3 P/C board.

With above signals restored, continue with diagnostics.

2. Check pins 20 and 21 at connector P1 for 5 volt, positive and negative pulses (M1C) with a width of 2 microseconds +2 pixel periods minimum. If these pulses are absent, repair the connecting cable or the controller A4 P/C board.

   If the M1 pulses are present, check that they also appear at the LSYN BNC jack on the camera rear panel. If they do not, repair the camera A2 board.

3. Check pins 20 and 23 at connector P1 for 5 volt, positive and negative pulses (EOF). The positive pulses (EOF+) should go true at the beginning, and false at the end of video line 100. If the pulses are absent, check the FSYN BNC jack on the camera rear panel. If the EOF pulses are present there, repair the camera A3 board. If they are also absent at the FSYN jack, continue with the next diagnostic step.

4. Check pins 19 and 20 of P3 on the camera A1 board for 5 volt, true ($\overline{\text{ØY1}}$) and false ($\overline{\text{ØY2}}$) pulses at 1/2 the camera line frequency. If they are incorrect or absent, repair the camera A2 P/C board. If they are present, continue with the next diagnostic step.

5. Check pins 23 and 24 of device U4 (Array) on the camera A1 board for 14 volt positive and negative pulses (ØY1, ØY2) at 1/2 the camera line frequency. If they are absent, repair the camera A1 P/C board.

   With the ØY1 and ØY2 signals restored, check pin 2 of device U4 for 6 volt negative pulses ($\overline{\text{EOF}}$), going false at the beginning, and true at the end of video line 100. If these pulses are not present, the Array, U4, may be defective. Return the A1 board to Reticon for further testing and/or repair.

   If the $\overline{\text{EOF}}$ pulses are present, but still do not appear at camera J4 or FSYN BNC connectors as required, check for these pulses at pin 8 of P3 on the A1 board. If present, repair A2 board. If not present, repair the A1 board.

With the MCLK, CCLK, M1, and EOF signals restored, check overall system operation, and continue diagnostics if necessary.

9.18 MC520 VIDEO

If the RS520 controller is not receiving Video from the camera, check the following signals with an oscilloscope.

1. Check pins 17 and 18 of P3 on the A1 board for 5 volt positive and negative $\overline{\text{ØY1}}$ and $\overline{\text{ØY2}}$ pulses at 1/2 the pixel frequency. If they are not present, repair the A2 board.

   If they are present, check pins 8/17/18, and 7/19/16 of device U4 (Array) for 14 volt positive and negative pulses at the same frequency. If they are not present, repair the A1 board. If they are present, continue diagnostics.

2. Check pin 15 of P3 on the camera A1 board for the same waveform as on pin 17. If not identical, repair the A2 board. If waveform is correct, check pin 5 of device U4 (Array) for identical waveform as on pin 8/17/18. If not identical, repair the A1 board.

3. Check pin 16 of P3 on the A1 board for 5 volt, negative pulses ($\overline{LT}$) with a pulse width of 2 microseconds + 2 pixel periods, minimum. This width is adjustable by S2 on the controller A4 board. (See Section VI.) If the signal is incorrect, repair the camera A2 board. If correct, check pin 21 of device U4 (Array) for 14 volt positive pulses (LT) with the same width as above. If signal is incorrect, repair the A1 board.

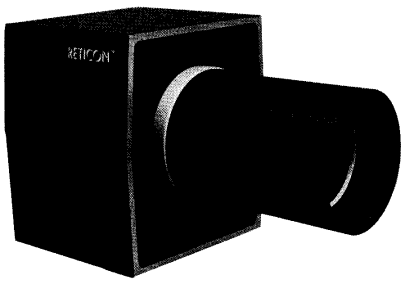
4. Check pins 2 and 4 at connector P1 on the A3 board for positive and negative 2 volt p-p video signals, averaging around ground level. If these signals are absent or incorrect, check TP1 on the camera A1 board for 2 volt p-p positive video averaging around + 7.5 volts nominal. If this signal is present, repair the A3 board, if this signal is not present, repair the A1 and/or A3 board, both may cause this fault since a feedback loop between the boards is involved.

   If the + 7.5 volt d-c level is present, but no video signal, check TP-2 and 3 on the A1 board for complementary square waves whose amplitude changes negatively with light saturation. If these signals are not present, the array may be faulty. Return the A1 board to Reticon for further testing and/or repair in this case.

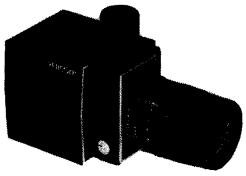
   Note: On cameras with Serial Numbers 78028 through 78045, TP2 and TP3 do not exist. Observe directly at pins 12 and 13 of device U4, the 100 x 100 array.

SECTION X

LIST OF ILLUSTRATIONS



MC520 C 100x100 Camera



MC520 V Camera
With Through-The-Lens Viewer

Figure 1

Figure No. 2

See Drawing 005-0081

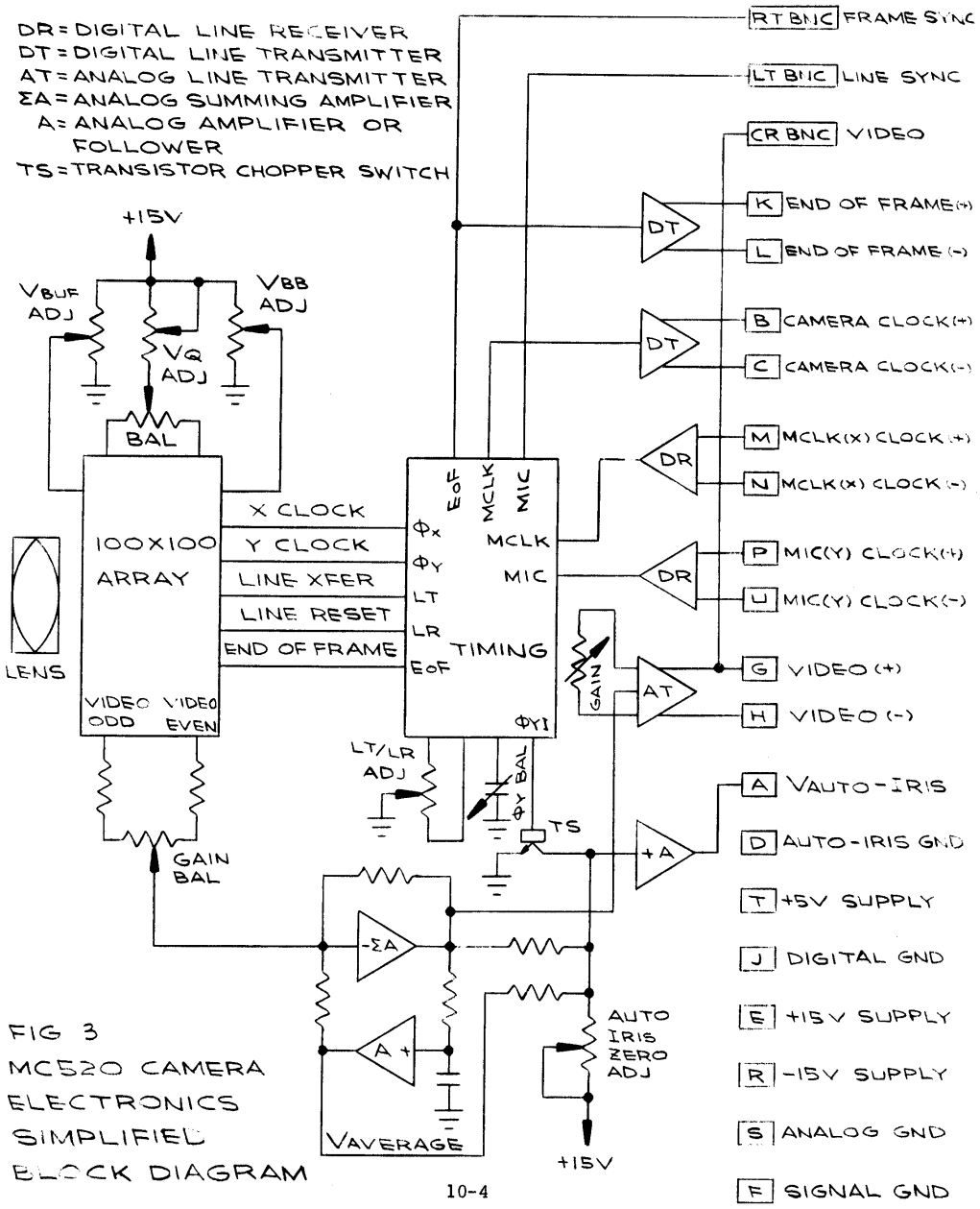
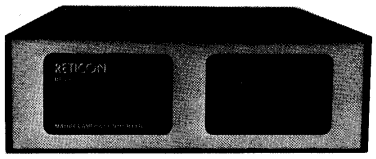
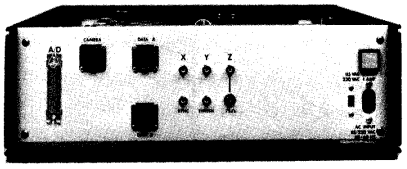


FIG 3
MC520 CAMERA ELECTRONICS SIMPLIFIED BLOCK DIAGRAM



RS520 Controller Front View

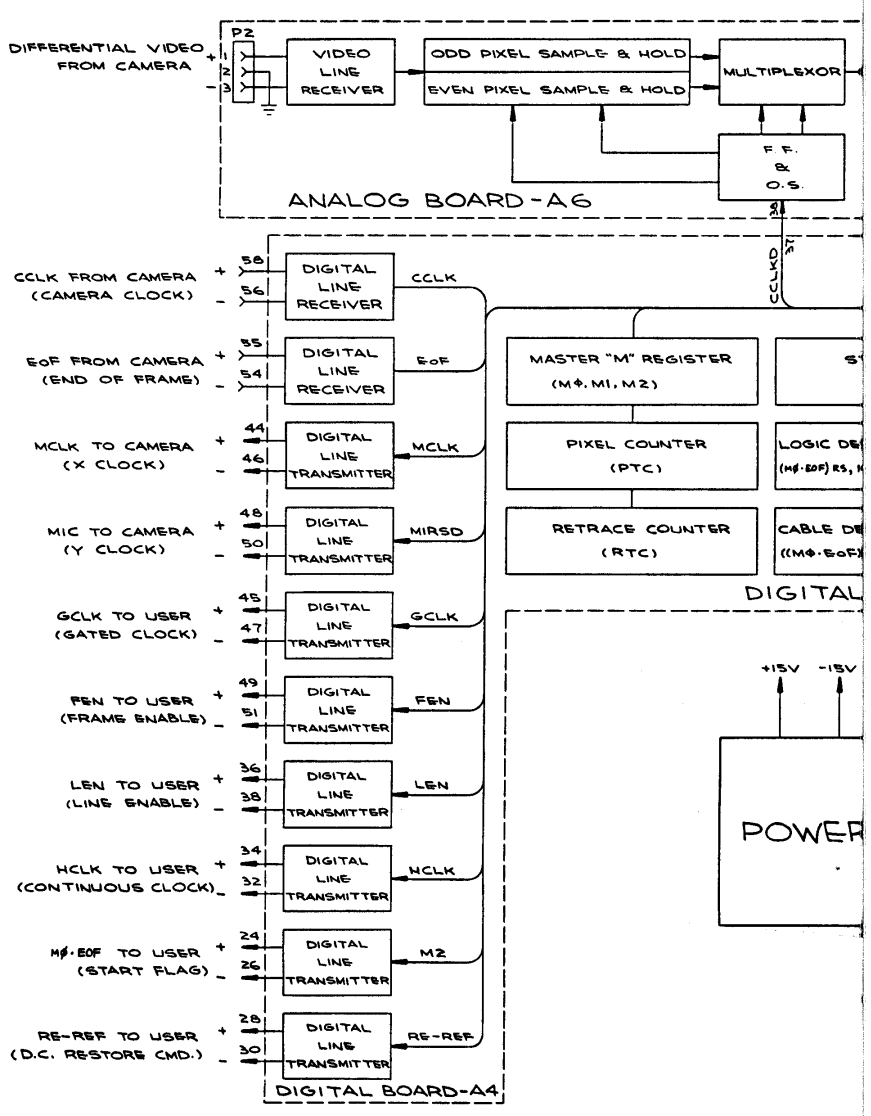


RS520 Controller Rear View

Figure 4

Figure No. 5

See Drawing 005-0082


DIFFERENTIAL VIDEO FROM CAMERA
P2
VIDEO LINE RECEIVER
ODD PIXEL SAMPLE & HOLD
EVEN PIXEL SAMPLE & HOLD
MULTIPLEXOR
F.F. & O.S.
ANALOG BOARD-A6
CCLK FROM CAMERA (CAMERA CLOCK)
EOF FROM CAMERA (END OF FRAME)
MCLK TO CAMERA (X CLOCK)
MIC TO CAMERA (Y CLOCK)
GCLK TO USER (GATED CLOCK)
FEN TO USER (FRAME ENABLE)
LEN TO USER (LINE ENABLE)
HCLK TO USER (CONTINUOUS CLOCK)
MΦ·EOF TO USER (START FLAG)
RE-REF TO USER (D.C. RESTORE CMD.)
DIGITAL LINE RECEIVER
DIGITAL LINE TRANSMITTER
CCLK
EOF
MCLK
MIRSD
GCLK
FEN
LEN
HCLK
M2
RE-REF
DIGITAL BOARD-A4
CCLKD
MASTER "M" REGISTER (MΦ, M1, M2)
PIXEL COUNTER (PTC)
RETRACE COUNTER (RTC)
DIGITAL
+15V
-15V
POWER

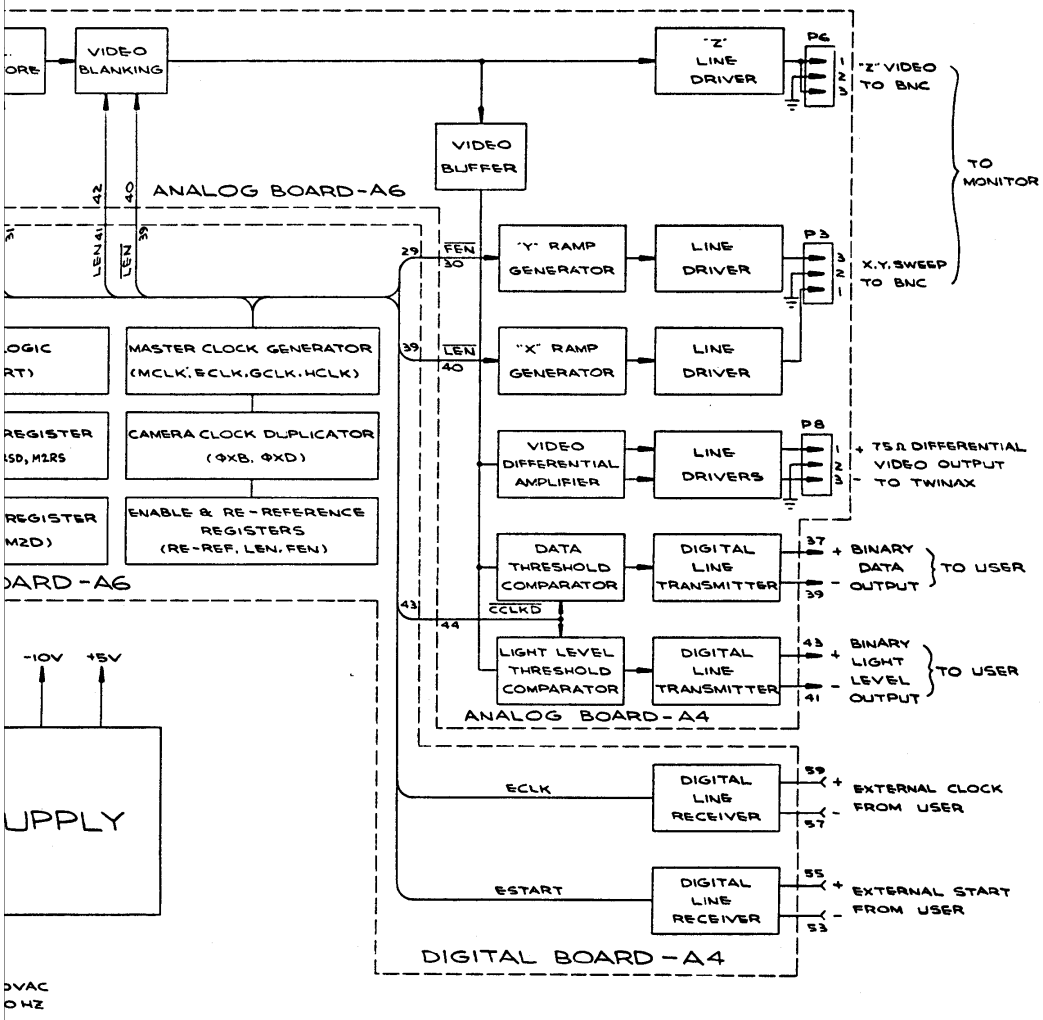


FIG 6
RS520 MATRIX CAMERA CONTROLLER ELECTRONICS.
SIMPLIFIED BLOCK DIAGRAM

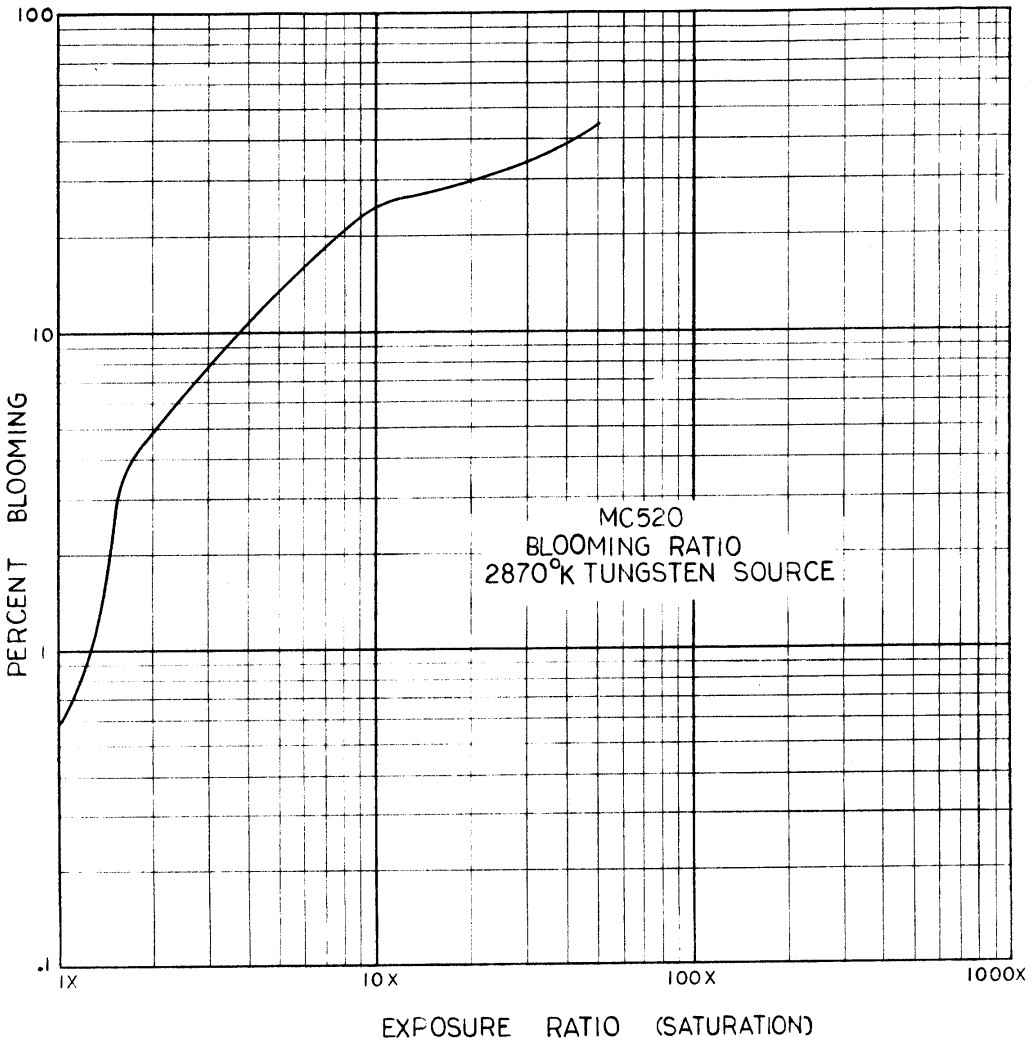

100
10
1
.1
PERCENT BLOOMING
MC520
BLOOMING RATIO
2870°K TUNGSTEN SOURCE
1X
10X
100X
1000X
EXPOSURE RATIO (SATURATION)

FIG. 8

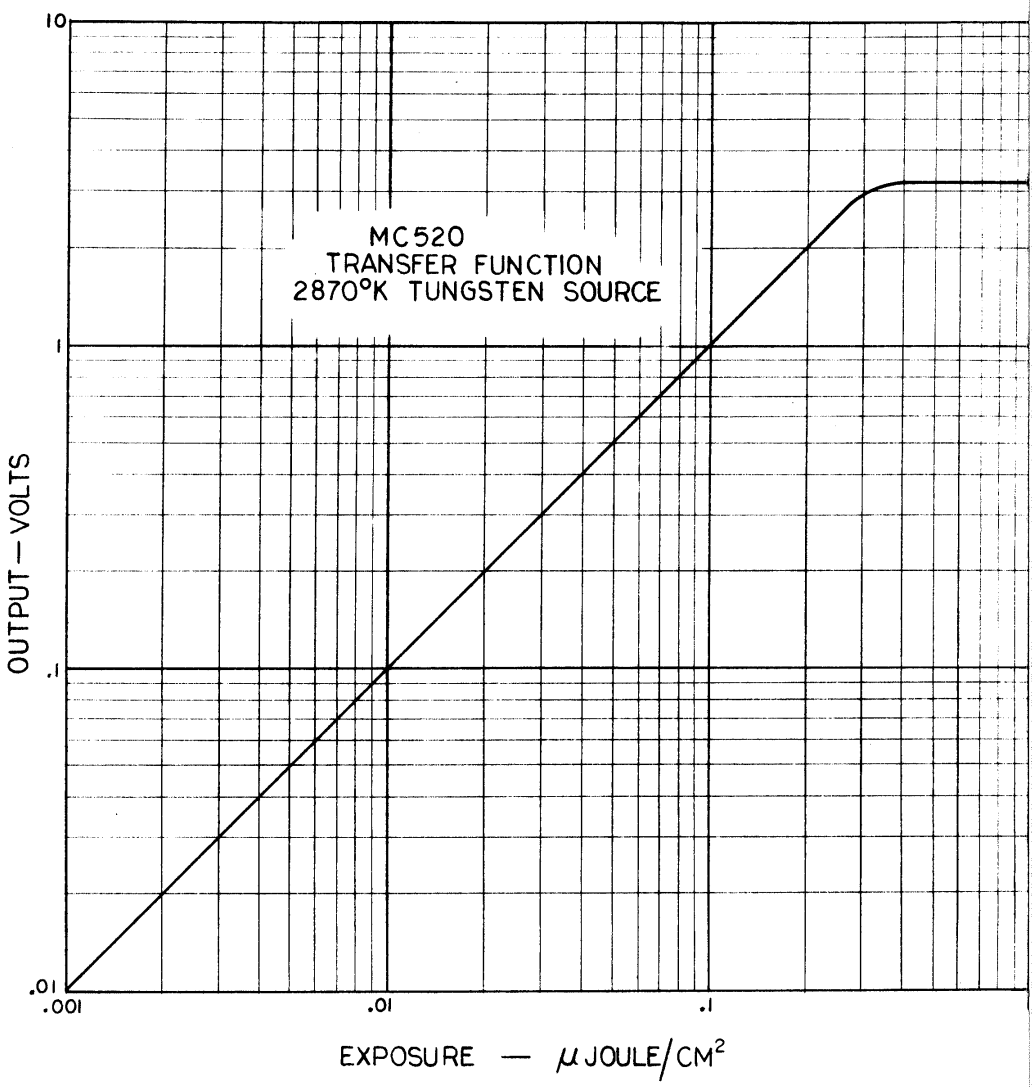
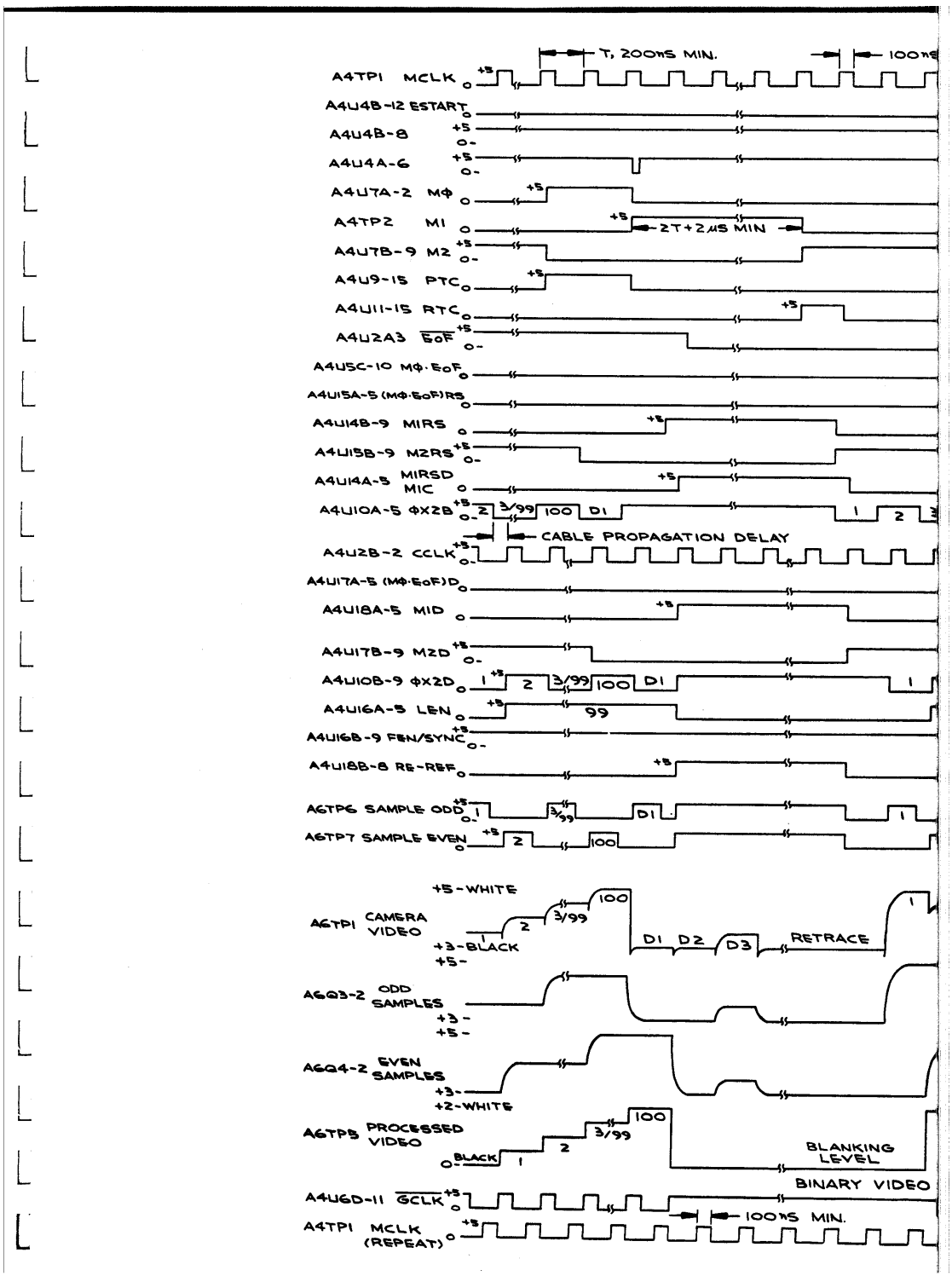

MC520
TRANSFER FUNCTION
2870°K TUNGSTEN SOURCE
OUTPUT — VOLTS
10
1
.1
.01
.001
.01
.1
EXPOSURE — μ JOULE/CM²

FIG. 7


T, 200nS MIN.
100nS
A4TP1 MCLK
A4U4B-12 ESTART
A4U4B-8
A4U4A-6
A4U7A-2 MΦ
A4TP2 MI
2T+2μS MIN
A4U7B-9 M2
A4U9-15 PTC
A4U11-15 RTC
A4U2A3 EOF
A4U5C-10 MΦ·EOF
A4U15A-5 (MΦ·EOF)RS
A4U14B-9 MIRS
A4U15B-9 M2RS
A4U14A-5 MIRSD MIC
A4U10A-5 ΦX2B
A4U2B-2 CCLK
CABLE PROPAGATION DELAY
A4U17A-5 (MΦ·EOF)D
A4U18A-5 MID
A4U17B-9 M2D
A4U10B-9 ΦX2D
A4U16A-5 LEN
A4U16B-9 FEN/SYNC
A4U18B-8 RE-REF
A6TP6 SAMPLE ODD
A6TP7 SAMPLE EVEN
A6TP1 CAMERA VIDEO
+5-WHITE
+3-BLACK
RETRACE
A6Q3-2 ODD SAMPLES
A6Q4-2 EVEN SAMPLES
+2-WHITE
A6TP5 PROCESSED VIDEO
BLACK
BLANKING LEVEL
BINARY VIDEO
A4U6D-11 GCLK
100nS MIN.
A4TP1 MCLK (REPEAT)

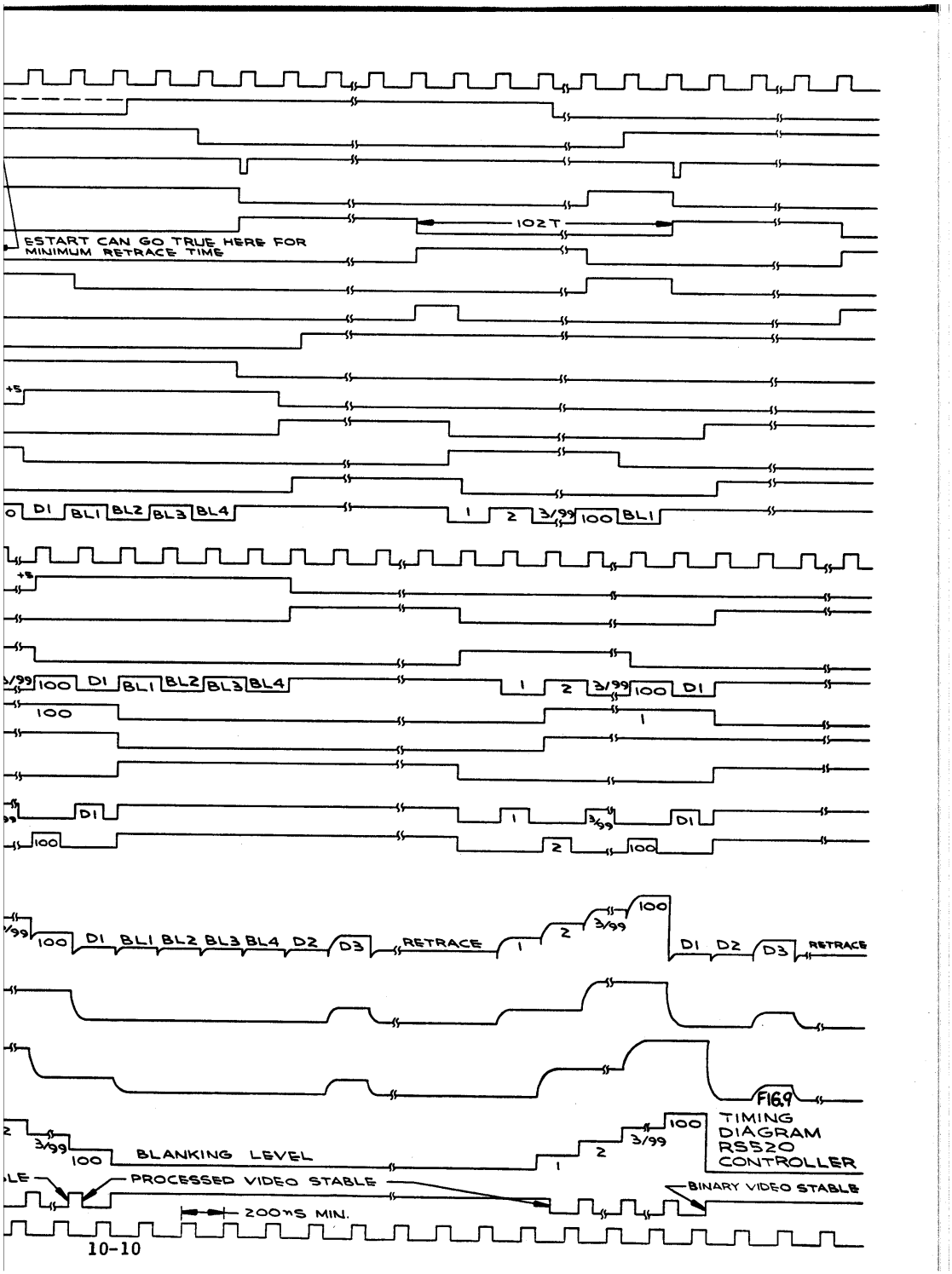


FIG.9 TIMING DIAGRAM RS520 CONTROLLER

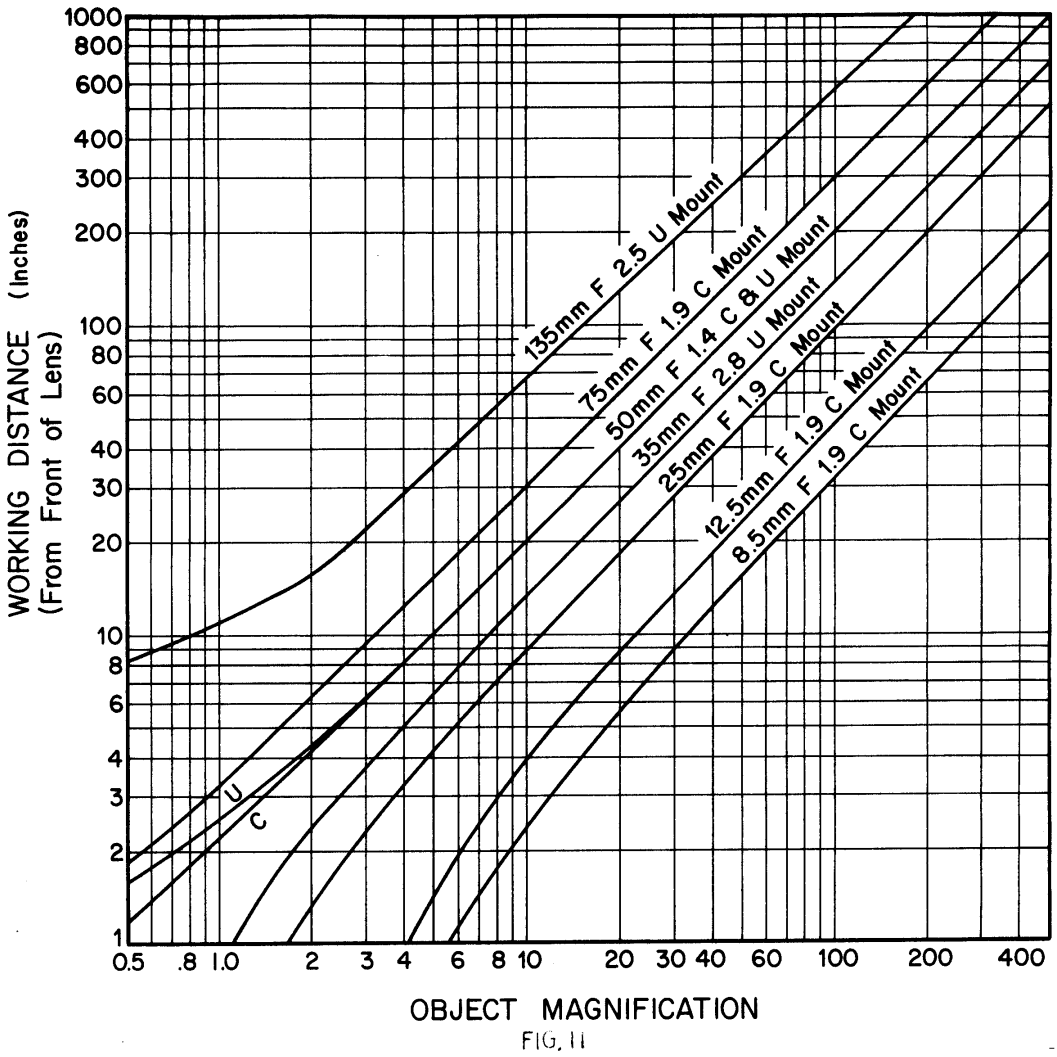
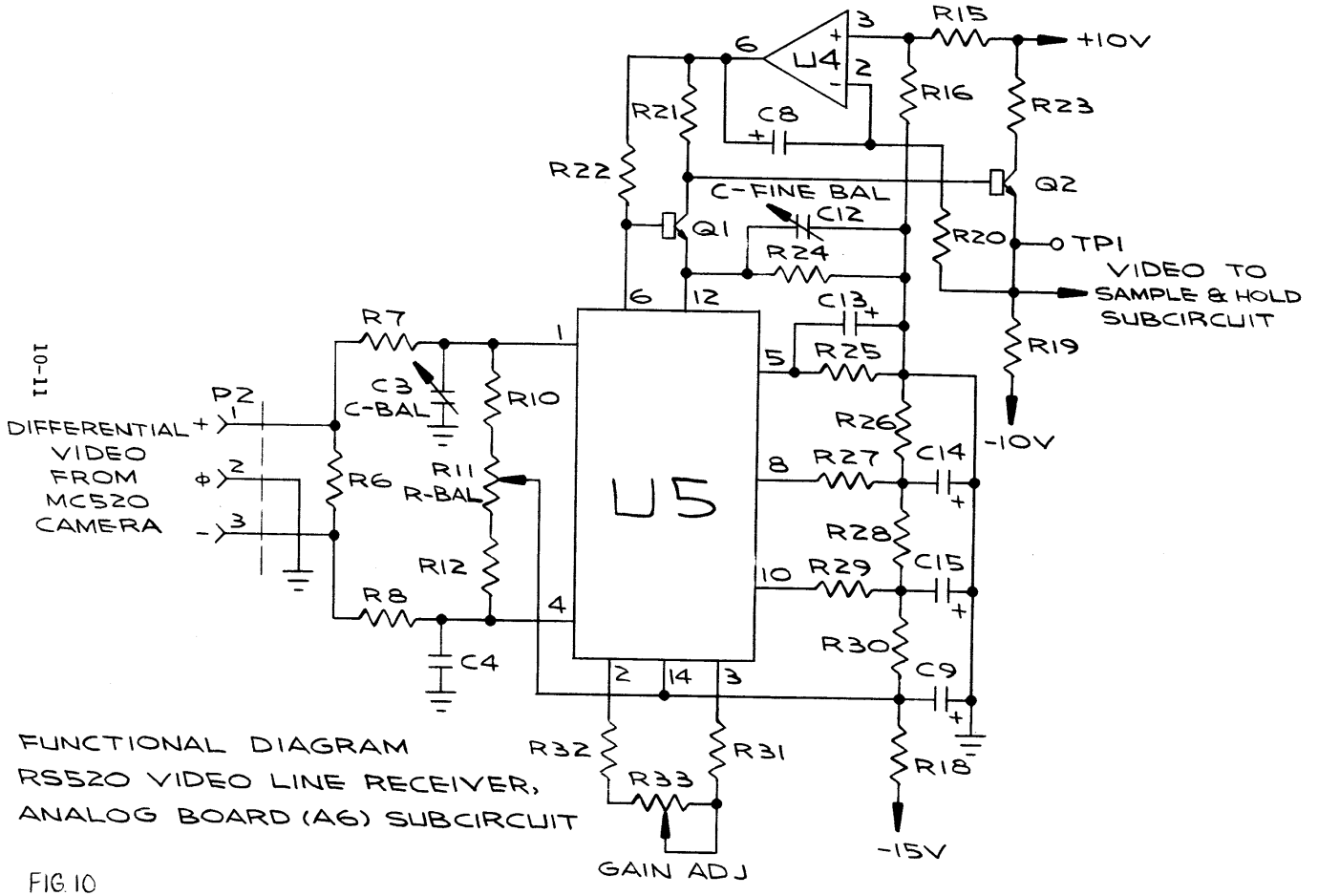

WORKING DISTANCE (Inches)
(From Front of Lens)
1000
800
600
400
300
200
100
80
60
40
30
20
10
8
6
4
3
2
1
0.5
.8
1.0
2
3
4
6
8
10
20
30
40
60
100
200
400
OBJECT MAGNIFICATION
135mm F 2.5 U Mount
75mm F 1.9 C Mount
50mm F 1.4 C & U Mount
35mm F 2.8 U Mount
25mm F 1.9 C Mount
12.5mm F 1.9 C Mount
8.5mm F 1.9 C Mount
U
C

FIG. 11



FUNCTIONAL DIAGRAM
RS520 VIDEO LINE RECEIVER,
ANALOG BOARD (A6) SUBCIRCUIT

FIG. 10

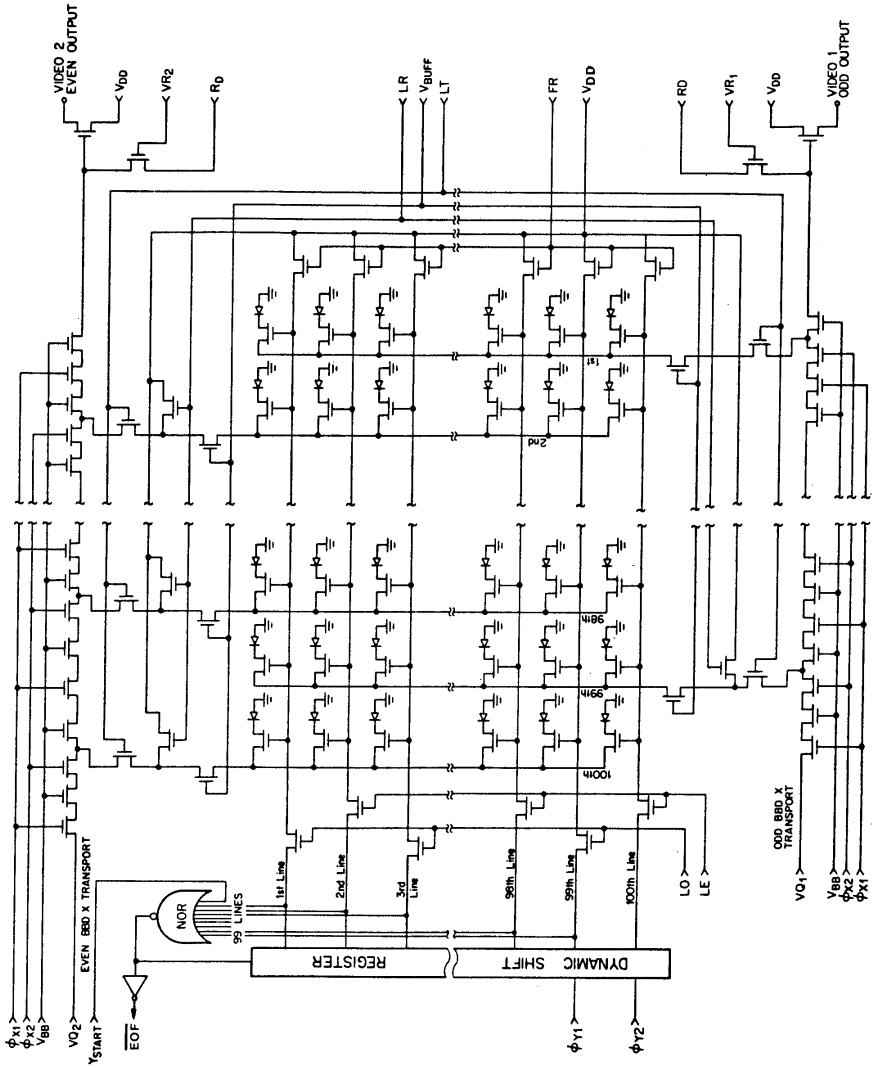

VIDEO 2 EVEN OUTPUT
V_{DD}
V_{R_2}
R_D
LR
V_{BUFF}
LT
FR
V_{DD}
RD
V_{R_1}
V_{DD}
VIDEO 1 ODD OUTPUT
1st
2nd
98th
99th
100th
1st Line
2nd Line
3rd Line
98th Line
99th Line
100th Line
LO
LE
ODD BBD X TRANSPORT
V_{Q_1}
V_{BB}
ϕ_{X2}
ϕ_{X1}
NOR
99 LINES
REGISTER
DYNAMIC SHIFT
EVEN BBD X TRANSPORT
ϕ_{X1}
ϕ_{X2}
V_{BB}
V_{Q_2}
Y_{START}
$\overline{EOF}$
ϕ_{Y1}
ϕ_{Y2}

FIG. 13

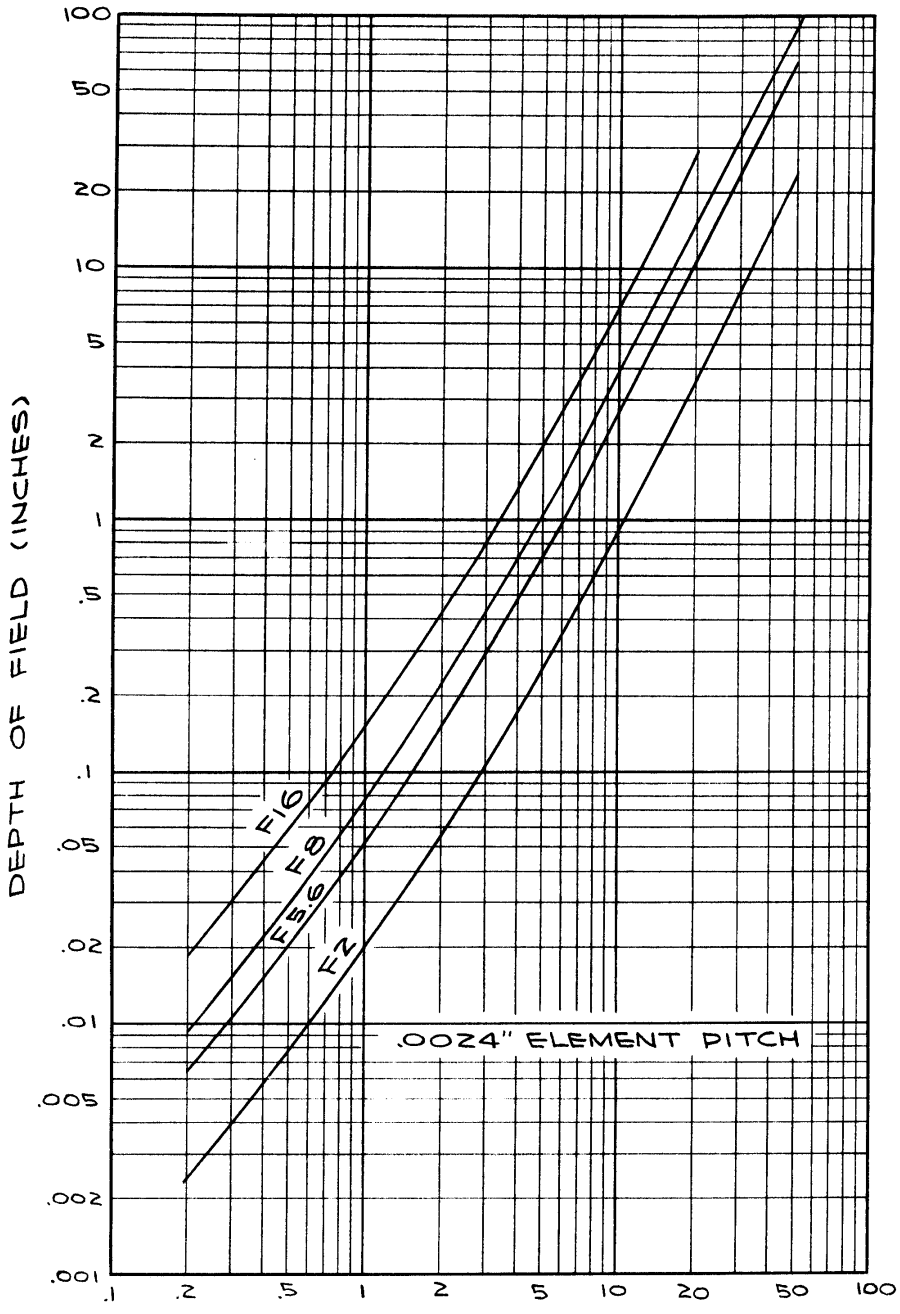
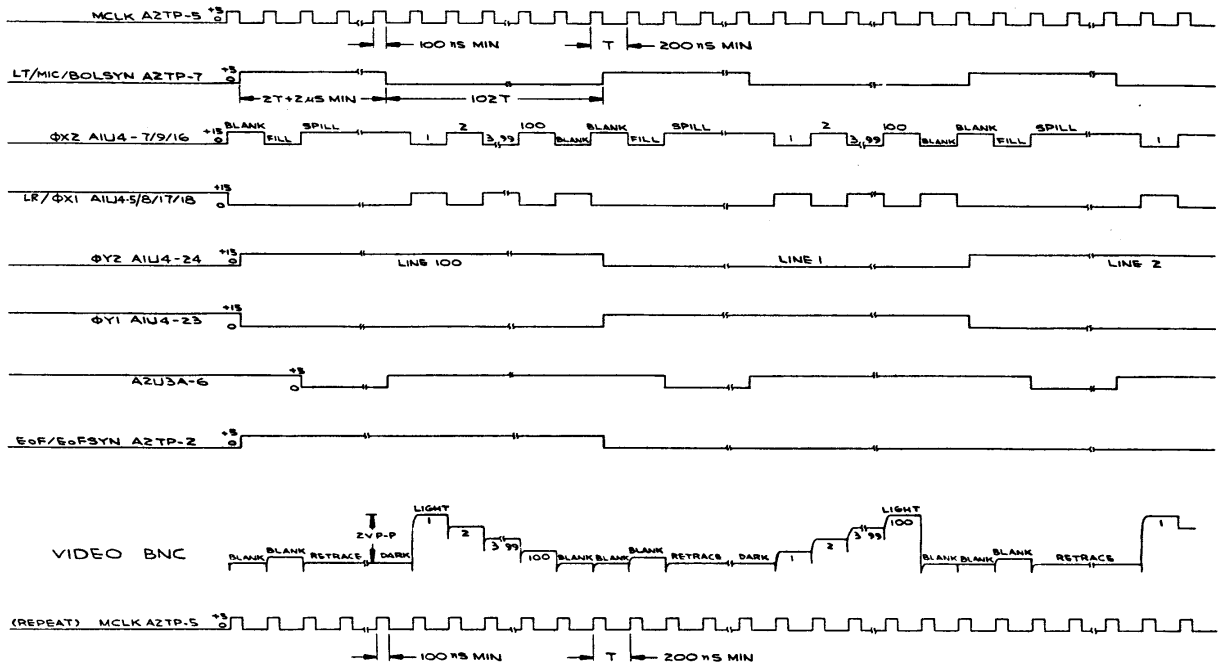

DEPTH OF FIELD (INCHES)
100
50
20
10
5
2
1
.5
.2
.1
.05
.02
.01
.005
.002
.001
.1
.2
.5
1
2
5
10
20
50
100
F16
F8
F5.6
F2
.0024" ELEMENT PITCH
OBJECT MAGNIFICATION

FIG. 12



EXAMPLE:

A2TP-5 = P/C CARD A2, TEST POINT 5.
A1U4-7/9/16 = P/C CARD A1, DEVICE U4, PIN 7, 9, AND 16.
A2U3A-6 = P/C CARD A2, DEVICE U3, CIRCUIT A, PIN 6.
WAVEFORMS ARE FOR SYNCHRONOUS OPERATION;
FOR ASYNCHRONOUS OPERATION SEE RS520
CONTROLLER TIMING DIAGRAMS.

TIMING DIAGRAM
MC520 CAMERA
FIG 15

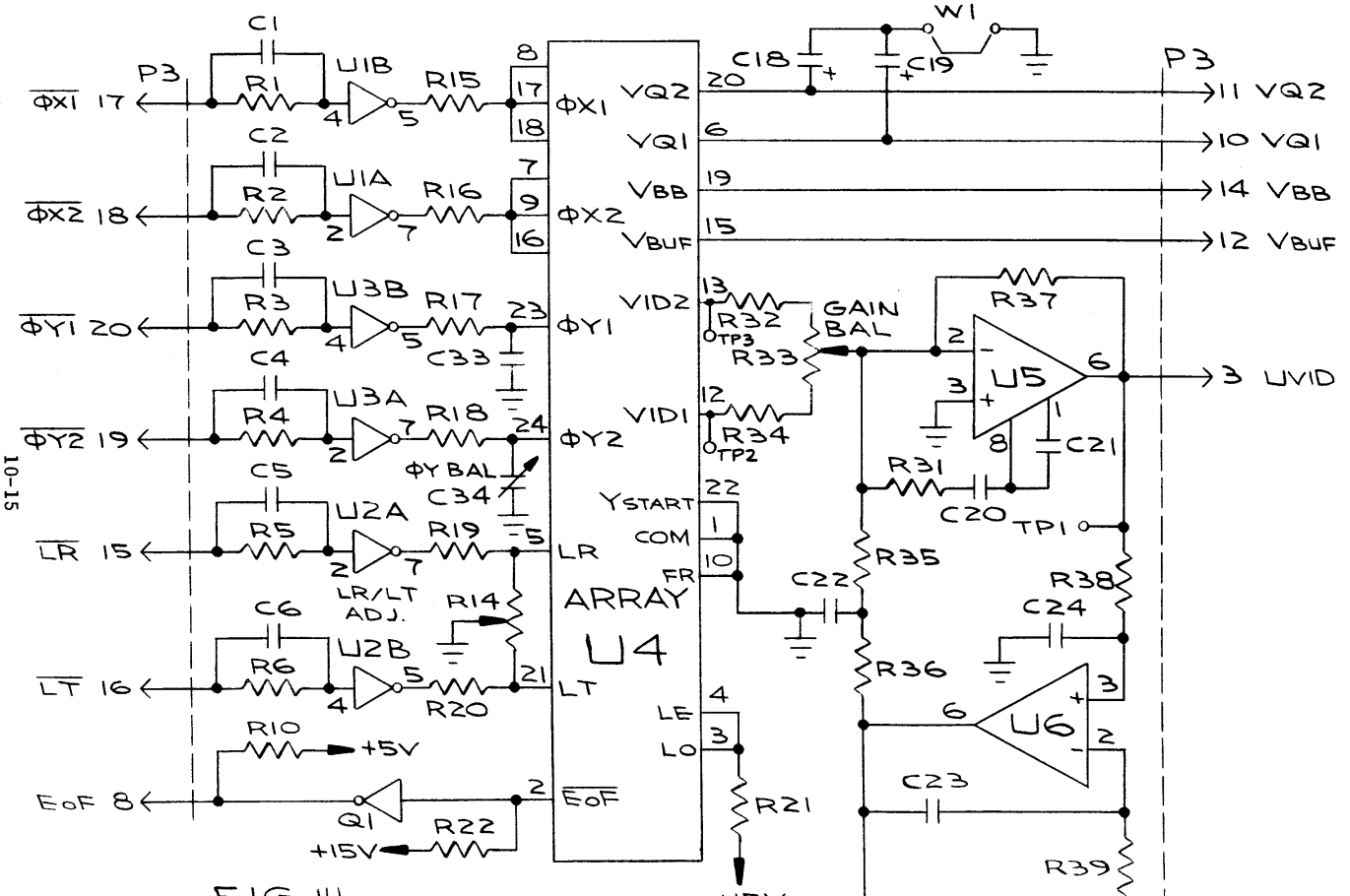
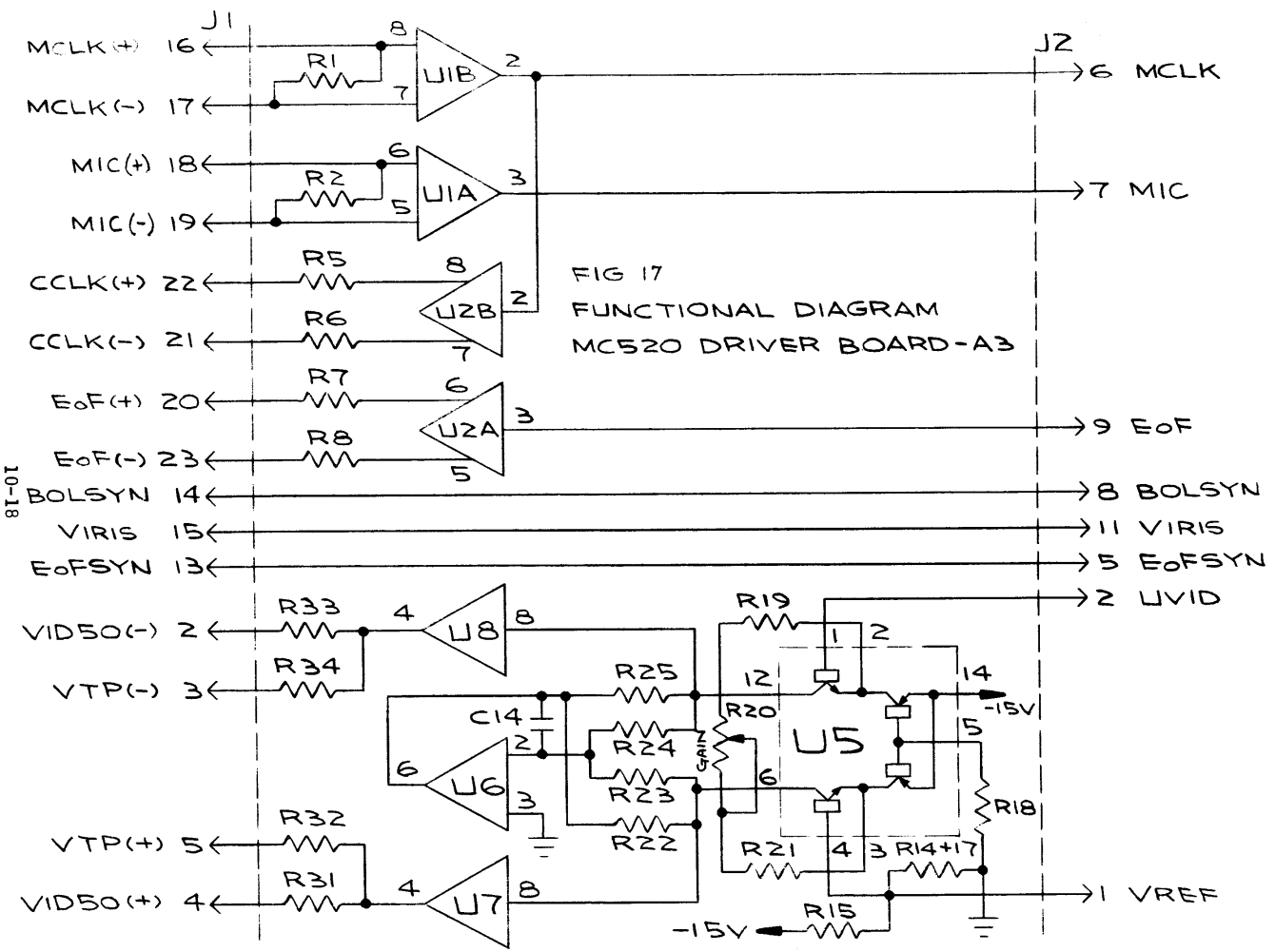


FIG 14
FUNCTIONAL DIAGRAM
MC520 ARRAY BOARD - A1


J1
J2
MCLK(+) 16
MCLK(-) 17
MIC(+) 18
MIC(-) 19
CCLK(+) 22
CCLK(-) 21
EoF(+) 20
EoF(-) 23
BOLSYN 14
VIRIS 15
EoFSYN 13
VID50(-) 2
VTP(-) 3
VTP(+) 5
VID50(+) 4
R1
R2
R5
R6
R7
R8
R33
R34
R32
R31
U1B
U1A
U2B
U2A
U8
U6
U7
U5
C14
R25
R24
R23
R22
R20
R19
R21
R18
R14+17
R15
GAIN
-15V
-15V
6 MCLK
7 MIC
9 EoF
8 BOLSYN
11 VIRIS
5 EoFSYN
2 UVID
1 VREF
FIG 17
FUNCTIONAL DIAGRAM
MC520 DRIVER BOARD-A3
10-18

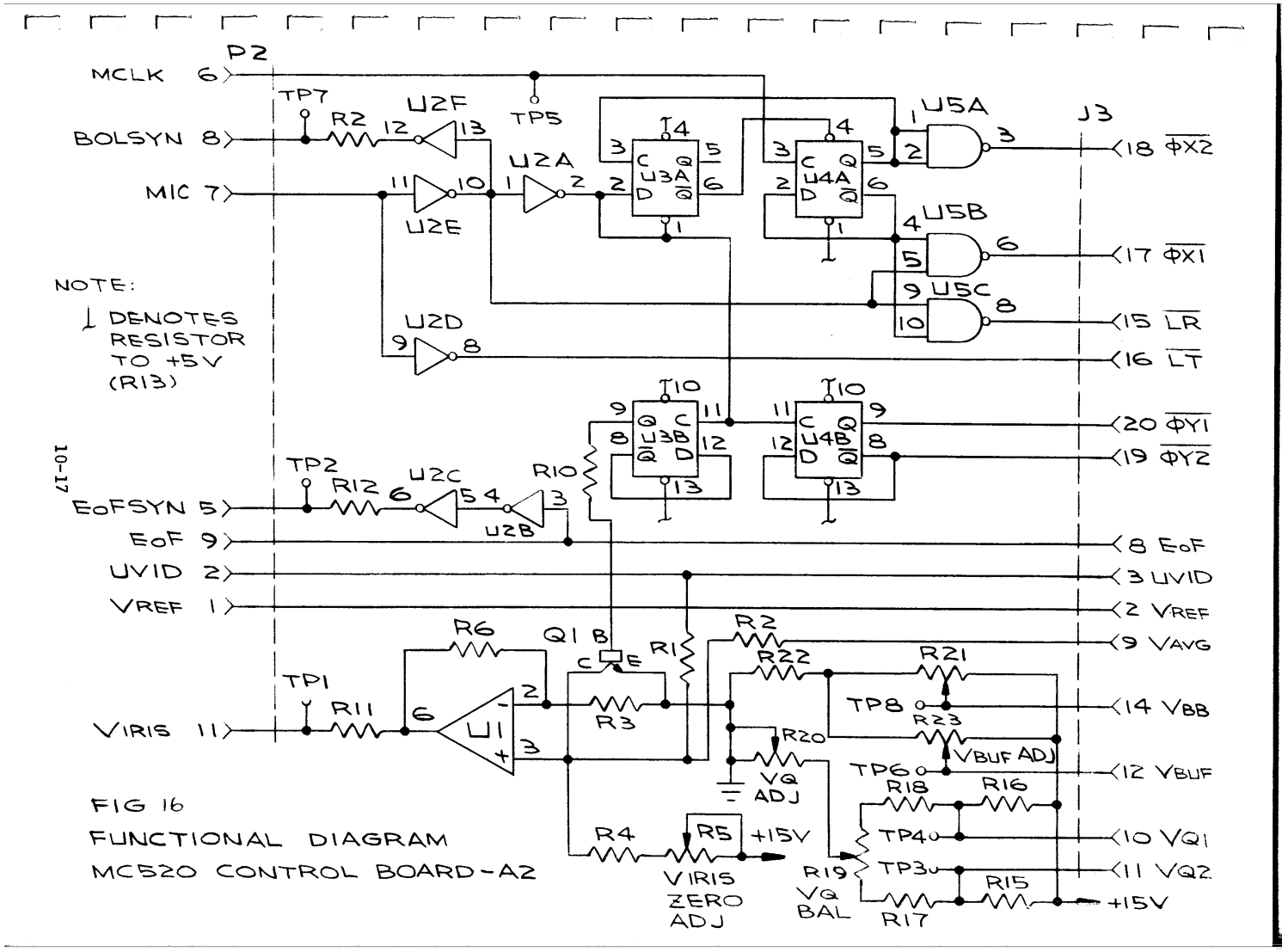


FIG 16
FUNCTIONAL DIAGRAM
MC520 CONTROL BOARD-A2

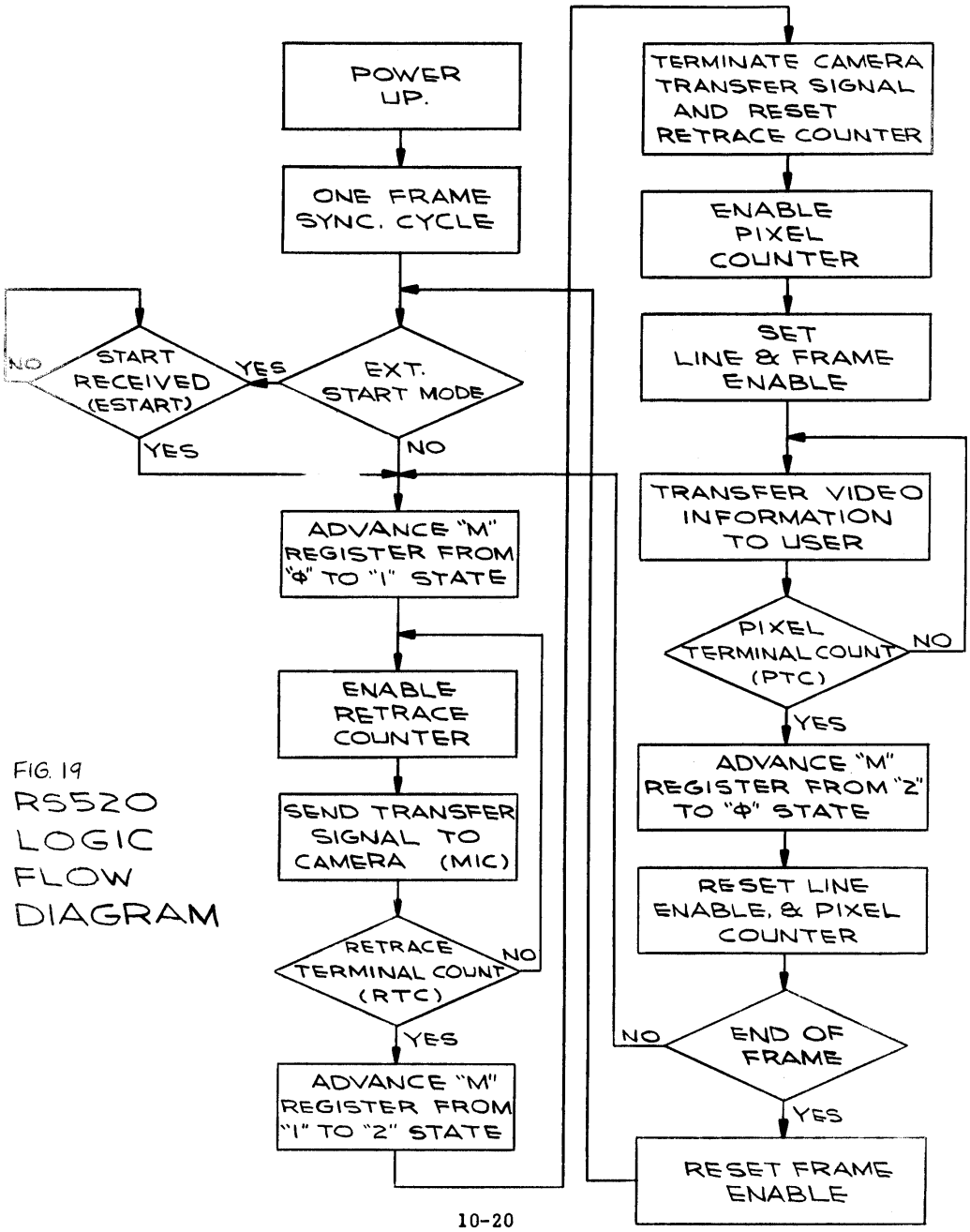


FIG. 19
RS520
LOGIC
FLOW
DIAGRAM

Figure 18

Not Used

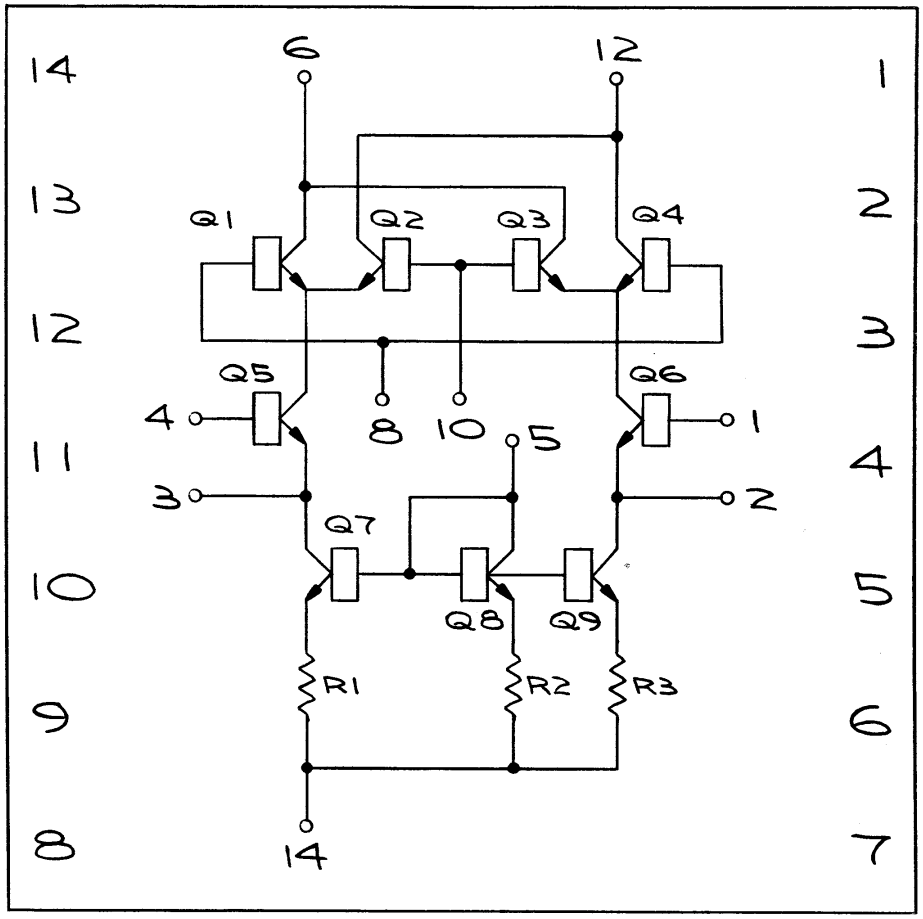


FIG. 21

BOTTOM VIEW
LM1496N-AMPLIFIER/SWITCH

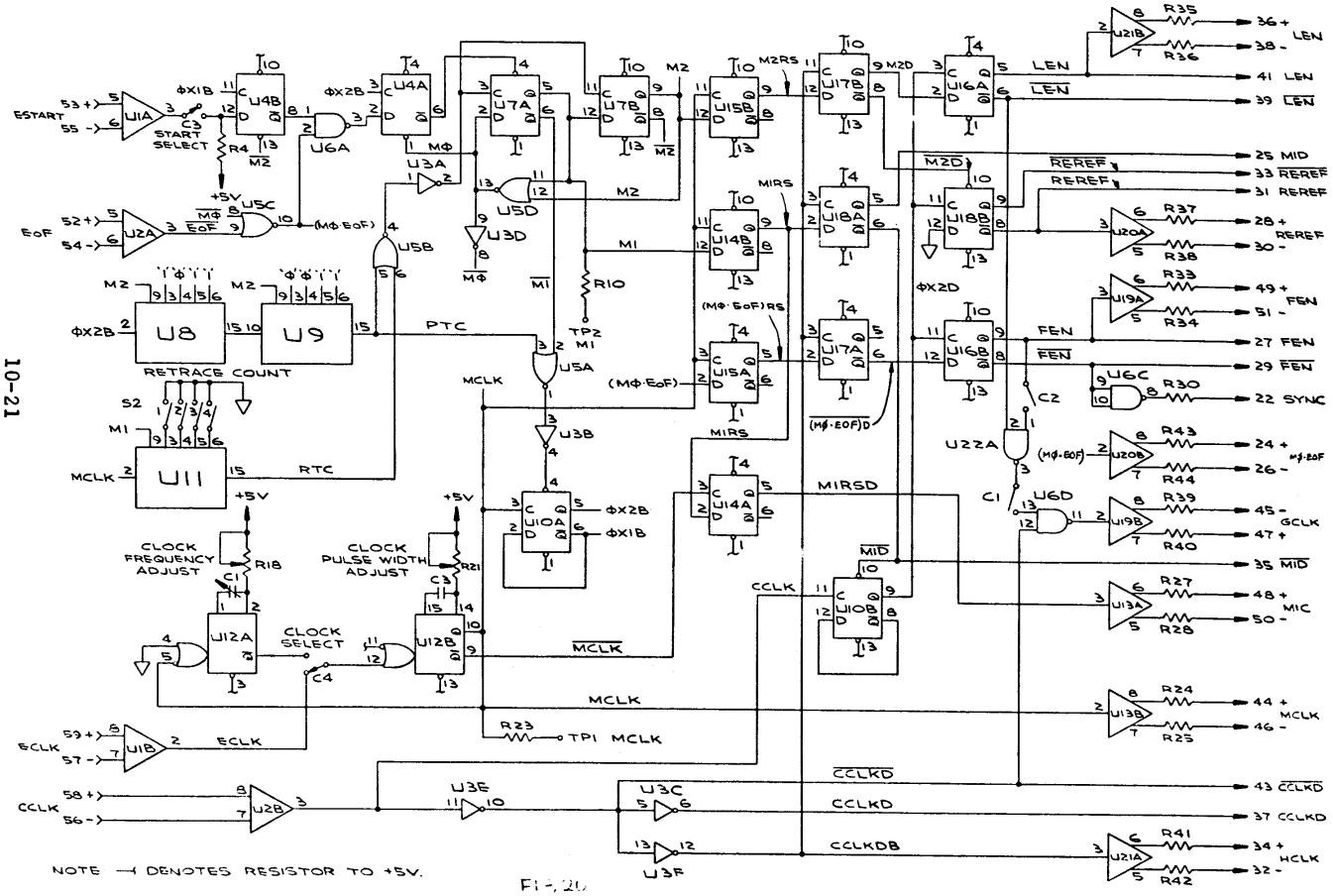


FIG. 20
FUNCTIONAL DIAGRAM
RS520 DIGITAL BOARD

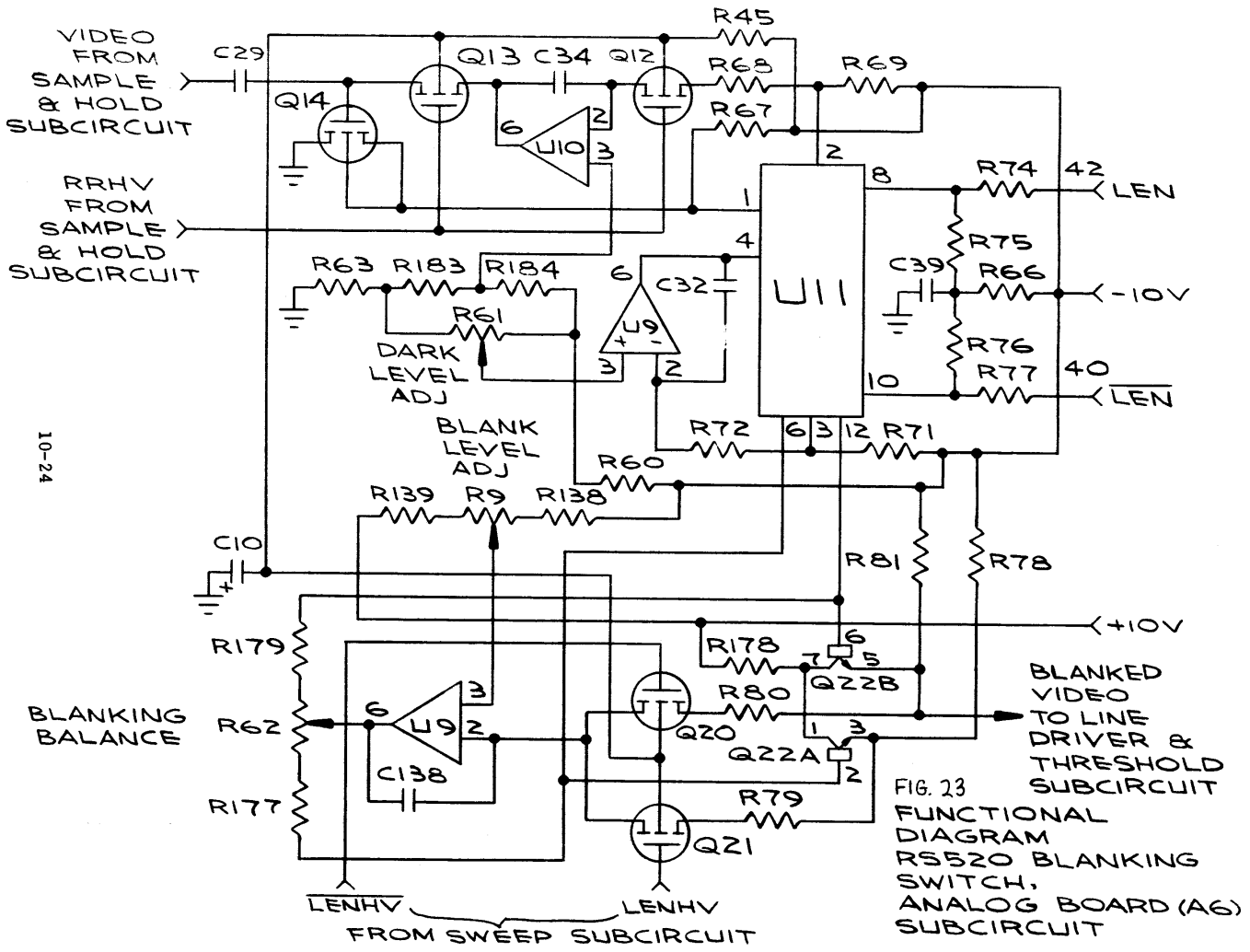


FIG. 23
FUNCTIONAL DIAGRAM RS520 BLANKING SWITCH, ANALOG BOARD (A6) SUBCIRCUIT

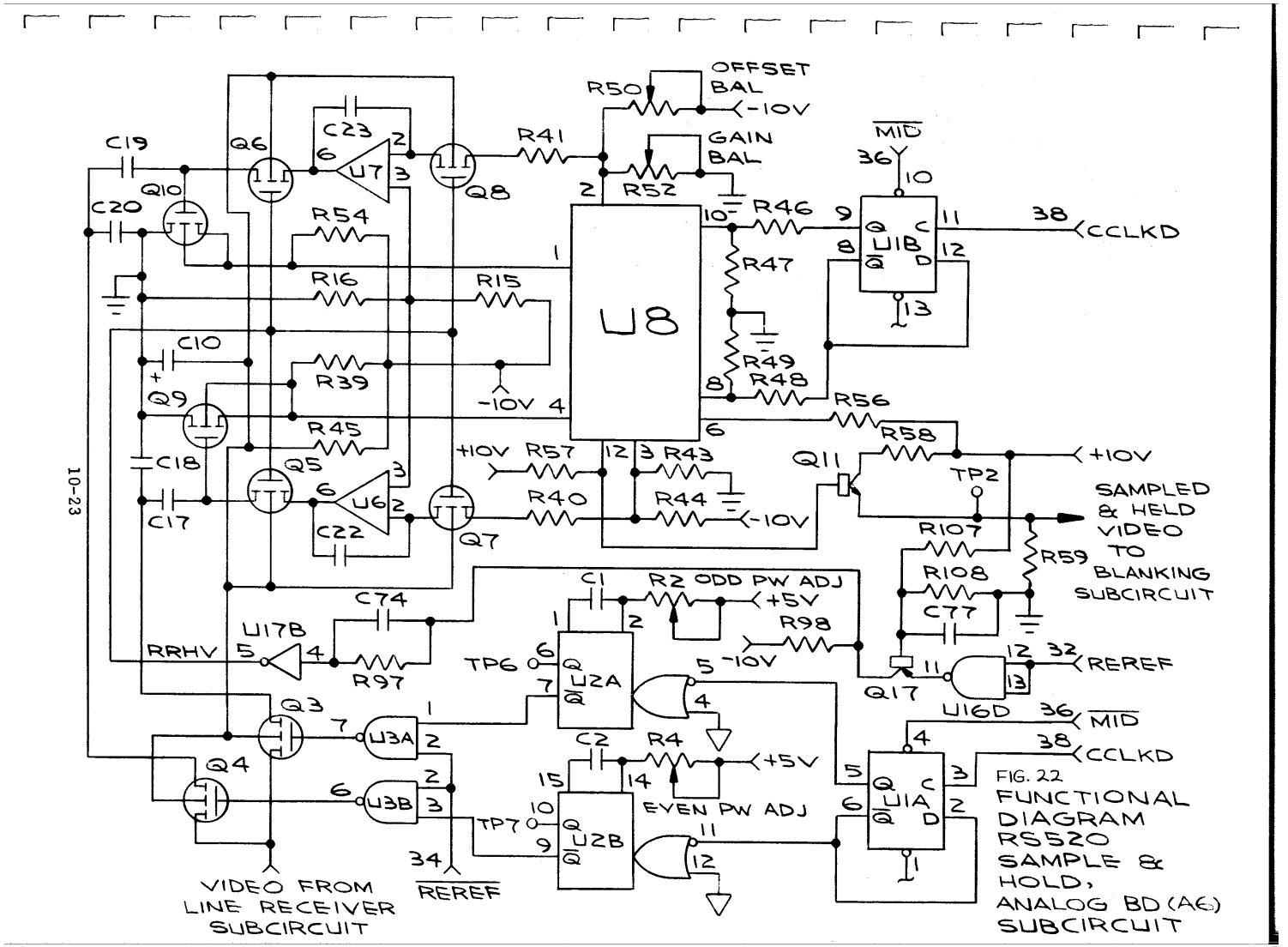
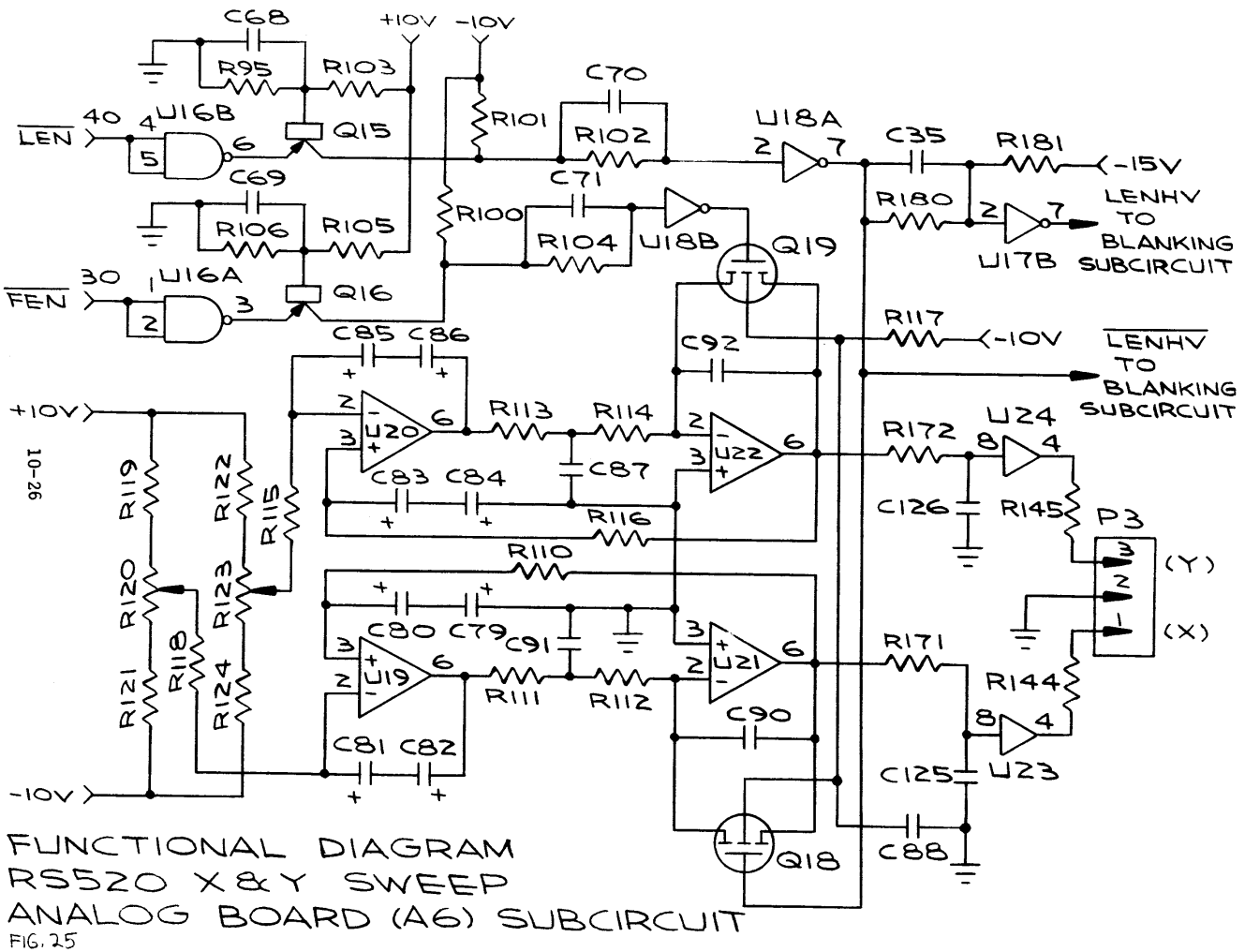
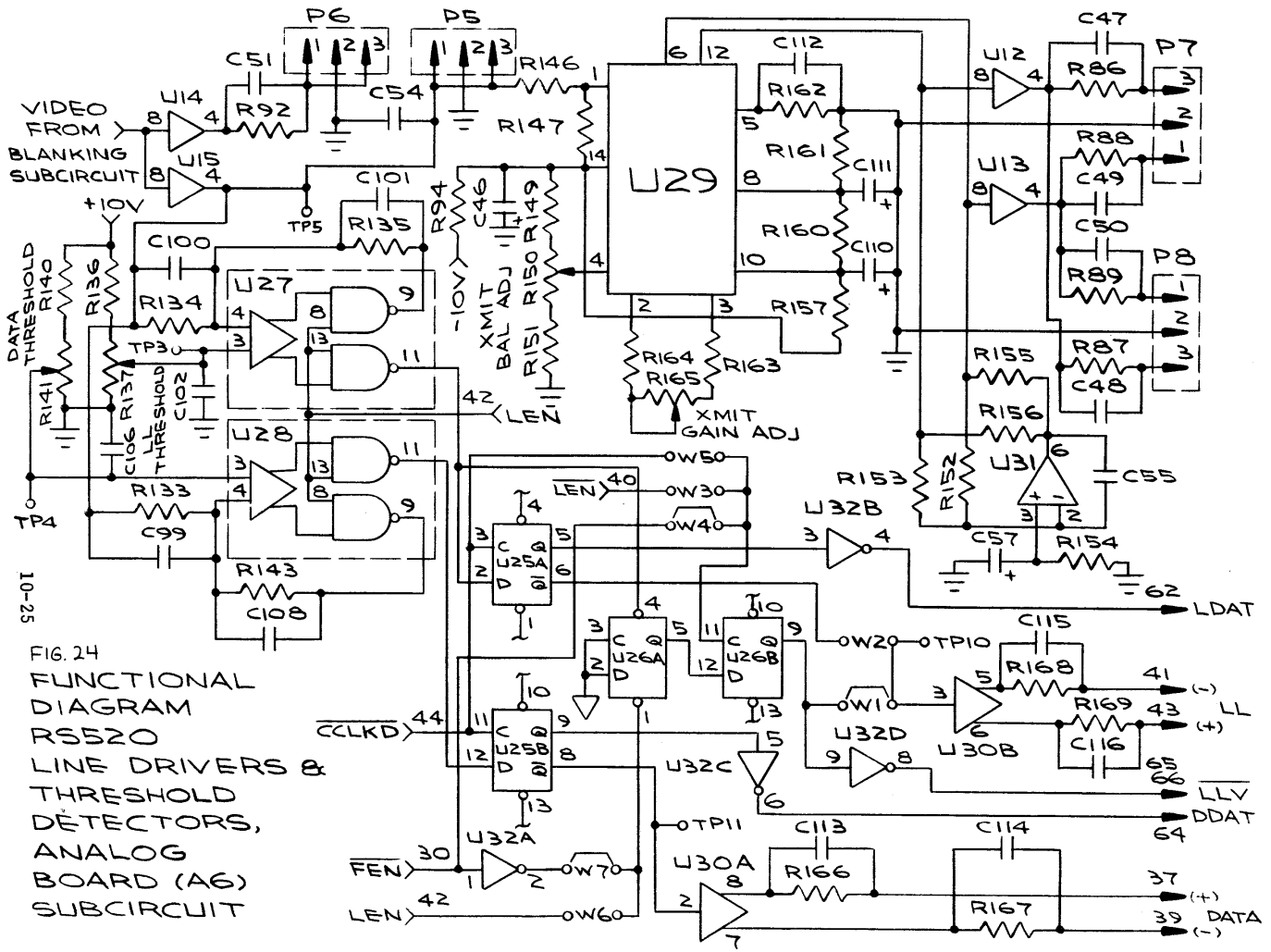


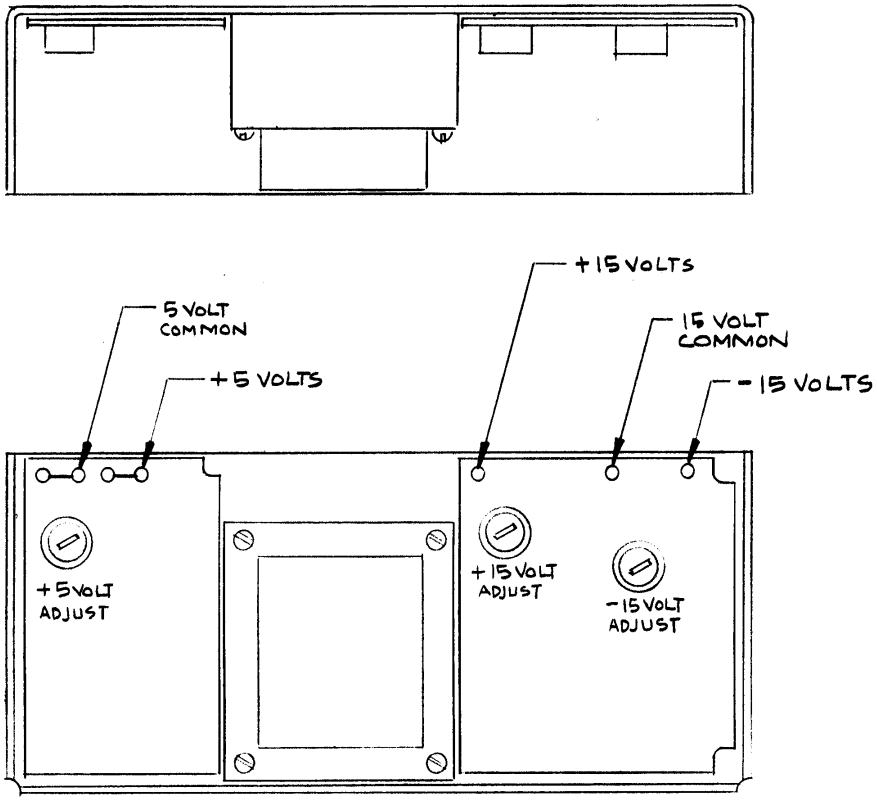
FIG. 22
FUNCTIONAL DIAGRAM RS520 SAMPLE & HOLD, ANALOG BD (A6) SUBCIRCUIT


C68
+10V
-10V
R95
R103
C70
40
U16B
LEN
Q15
R101
R102
U18A
C35
R181
-15V
C69
C71
R180
LENHV
TO
BLANKING
SUBCIRCUIT
R106
R105
R100
R104
U18B
Q19
U17B
30
U16A
FEN
Q16
R117
-10V
LENHV
TO
BLANKING
SUBCIRCUIT
C85
C86
C92
+10V
U20
R113
R114
U22
U24
R172
10-26
R119
R122
R115
C83
C84
C87
C126
R145
P3
R116
R110
R120
R123
C80
C79
C91
(Y)
(X)
R121
R118
R124
U19
R111
R112
U21
R171
R144
C90
C81
C82
U23
C125
-10V
Q18
C88
FUNCTIONAL DIAGRAM
RS520 X&Y SWEEP
ANALOG BOARD (A6) SUBCIRCUIT
FIG. 25



10-25

FIG. 24
FUNCTIONAL DIAGRAM RS520 LINE DRIVERS & THRESHOLD DETECTORS, ANALOG BOARD (A6) SUBCIRCUIT

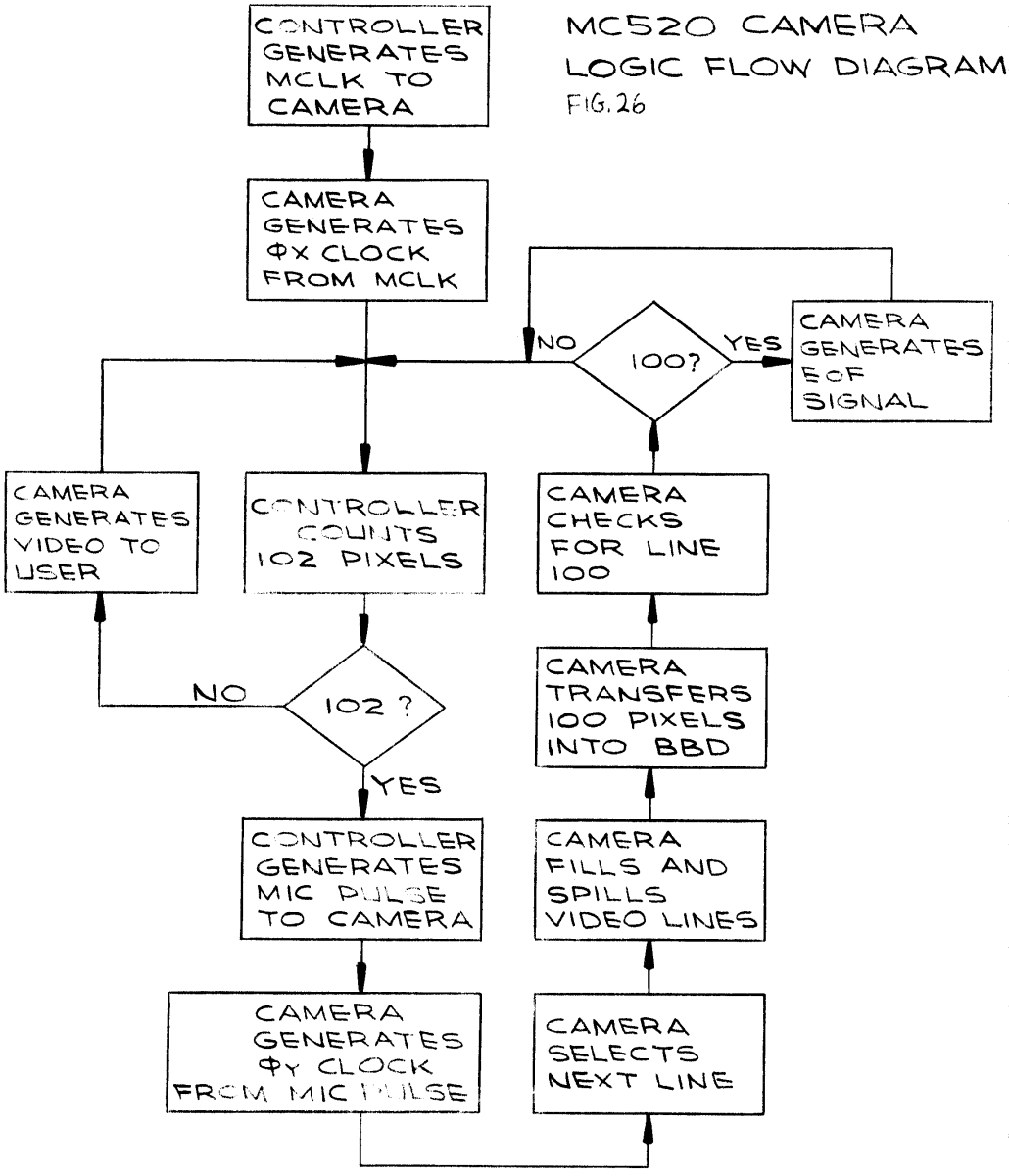


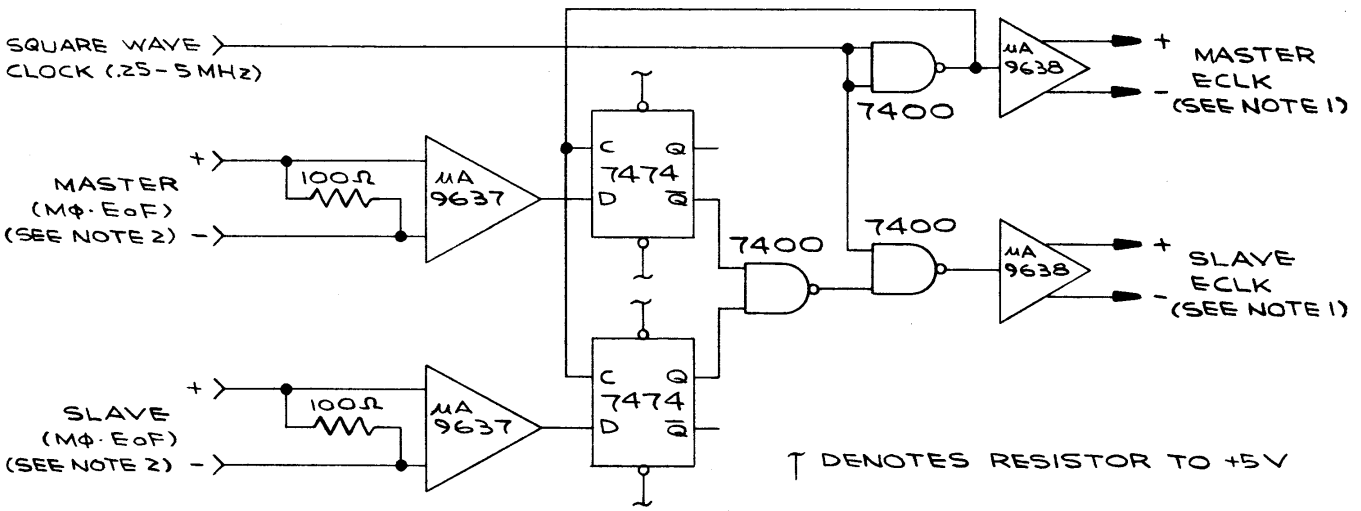
RS 520 POWER SUPPLY
ADJUSTMENT AND
OUTPUT TERMINAL LOCATION

FIG. 27

MC520 CAMERA LOGIC FLOW DIAGRAM

FIG. 26





10-30

NOTES:

1. ECLK CONNECTIONS TO CONTROLLER DATA A CONNECTOR PINS E(+), F(-).
2. (MΦ·EoF) CONNECTIONS TO CONTROLLER DATA B CONNECTOR PINS P(+), U(-). IN CONTROLLERS WITH SERIAL Nº'S 78083 TO 78091, JUMPER W10 ON THE A4 BOARD MUST BE CUT AND A WIRE RUN FROM PIN 2 OF DEVICE U15A TO PIN 2 OF DEVICE U20B. THIS CHANGE BRINGS OUT (MΦ·EoF) INSTEAD OF M2.
3. BOTH CONTROLLERS SET FOR EXTERNAL CLOCK, AND INTERNAL OR EXTERNAL START AS REQUIRED FOR APPLICATION.

FIG 29 LOGIC FOR MASTER-SLAVE OPERATION OF MULTIPLE CAMERAS.

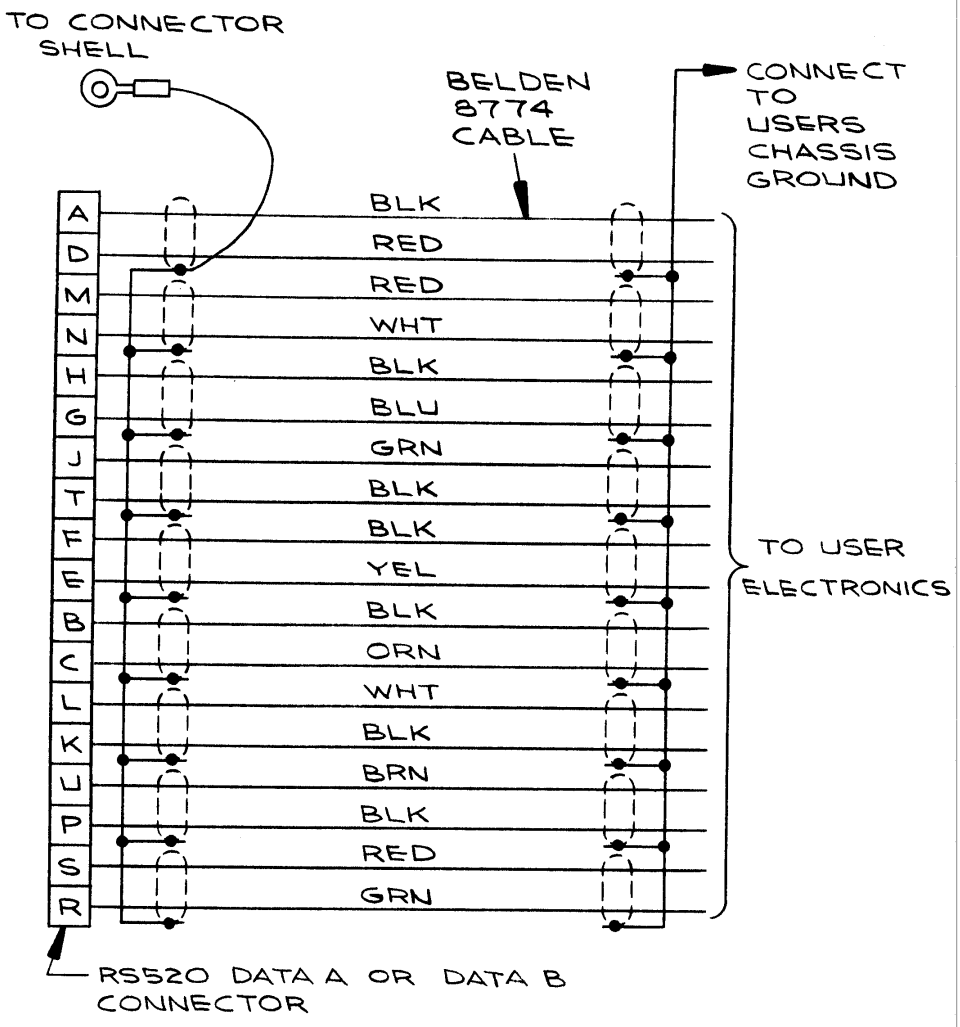
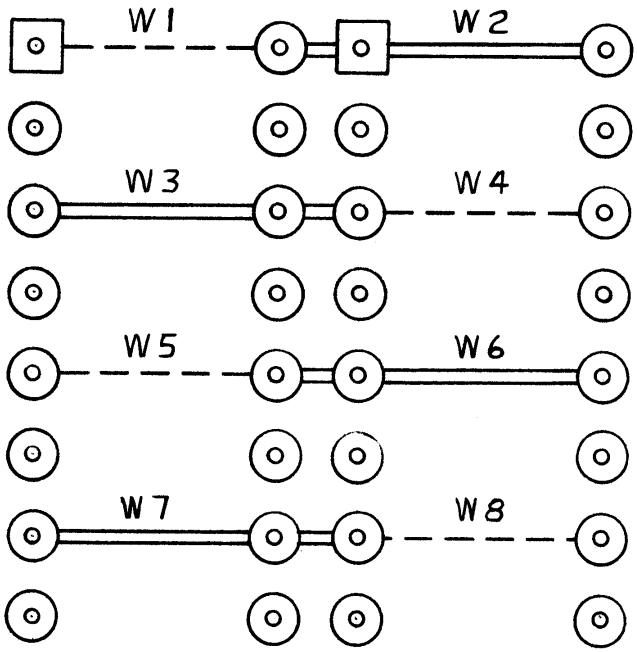


FIG 28
USER WIRING FOR DATA A & DATA B CONNECTORS

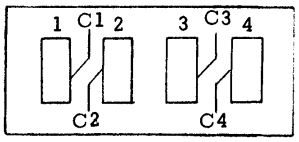


PIXEL BLANKING, JUMPER CONFIGURATION

FIG. 30

TABLE I

S1 SWITCH SETTINGS



S1 - Front View

C1 & C2 operate together to control the GCLK output as follows:

1. With C1 rocker depressed toward number 1, continuous GCLK is selected regardless of C2 position.
2. With C1 depressed away from number 1 and C2 depressed toward number 2, GCLK is disabled during all retrace intervals, i.e., GCLK pulses will occur only for active pixels.
3. With C1 depressed away from number 1 and C2 depressed away from number 2, GCLK is disabled during all retrace intervals except single retrace interval between end of line 100 and beginning of line 1.

C3 controls the camera Start mode as follows:

1. With C3 rocker depressed toward number 3, external Start mode is selected.
2. With C3 depressed away from number 3, internal Start mode is selected.

C4 controls the camera clocking mode as follows:

1. With C4 rocker depressed toward number 4, external Clock mode is selected.
2. With C4 depressed away from number 4, internal Clock mode is selected.

NOTE: IF C4 IS ACTUATED FROM INTERNAL TO EXTERNAL AND BACK TO INTERNAL CLOCK POSITION, INTERNAL CLOCK WILL NOT START UNTIL SYSTEM POWER IS TURNED OFF AND BACK ON.

SECTION XI

LIST OF TABLES

TABLE III

LIGHT LEVEL JUMPER OPTIONS

JUMPERS INSTALLED	BINARY OUTPUT RESPONSE AT DATA A I/O CONNECTOR
W1 & W3 & W6	GOES TRUE OR REMAINS TRUE AT THE END OF ANY LINE IN WHICH A PIXEL EXCEEDS THRESHOLD. GOES FALSE AT THE END OF THE FIRST FOLLOWING LINE IN WHICH A PIXEL DOES NOT EXCEED THRESHOLD.
W1 & W4 & W6	GOES TRUE OR REMAINS TRUE AT THE END OF ANY FRAME IN WHICH A PIXEL EXCEEDS THRESHOLD. GOES FALSE AT THE END OF THE FIRST FOLLOWING LINE IN WHICH A PIXEL DOES NOT EXCEED THRESHOLD.
W1 & W5 & W6	GOES TRUE OR REMAINS TRUE WHEN A PIXEL EXCEEDS THRESHOLD. GOES FALSE AT THE END OF THE FIRST FOLLOWING LINE THAT A PIXEL DOES NOT EXCEED THRESHOLD.
W1 & W3 & W7	GOES TRUE OR REMAINS TRUE AT THE END OF ANY LINE IN WHICH A PIXEL EXCEEDS THRESHOLD. GOES FALSE AT THE END OF THE FIRST FOLLOWING FRAME IN WHICH A PIXEL DOES NOT EXCEED THRESHOLD.
W1 & W4 & W7	GOES TRUE OR REMAINS TRUE AT THE END OF ANY FRAME IN WHICH A PIXEL EXCEEDS THRESHOLD. GOES FALSE AT THE END OF THE FIRST FOLLOWING FRAME IN WHICH A PIXEL DOES NOT EXCEED THRESHOLD.
W1 & W5 & W7	GOES TRUE OR REMAINS TRUE WHEN A PIXEL EXCEEDS THRESHOLD. GOES FALSE AT THE END OF THE FIRST FOLLOWING FRAME IN WHICH A PIXEL DOES NOT EXCEED THRESHOLD.

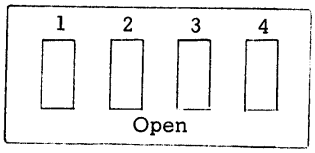
If Jumper W2 is installed instead of W1, TP10 on the A6 board will respond to the Light Level Threshold in the same manner that TP11 responds to the Data Threshold. The Light Level indicator on the controller front panel will, however, continue to respond as determined by the "Jumpers Installed" table above for W3 through W7.

TABLE II

RETRACE COUNT SWITCH SETTINGS - S2

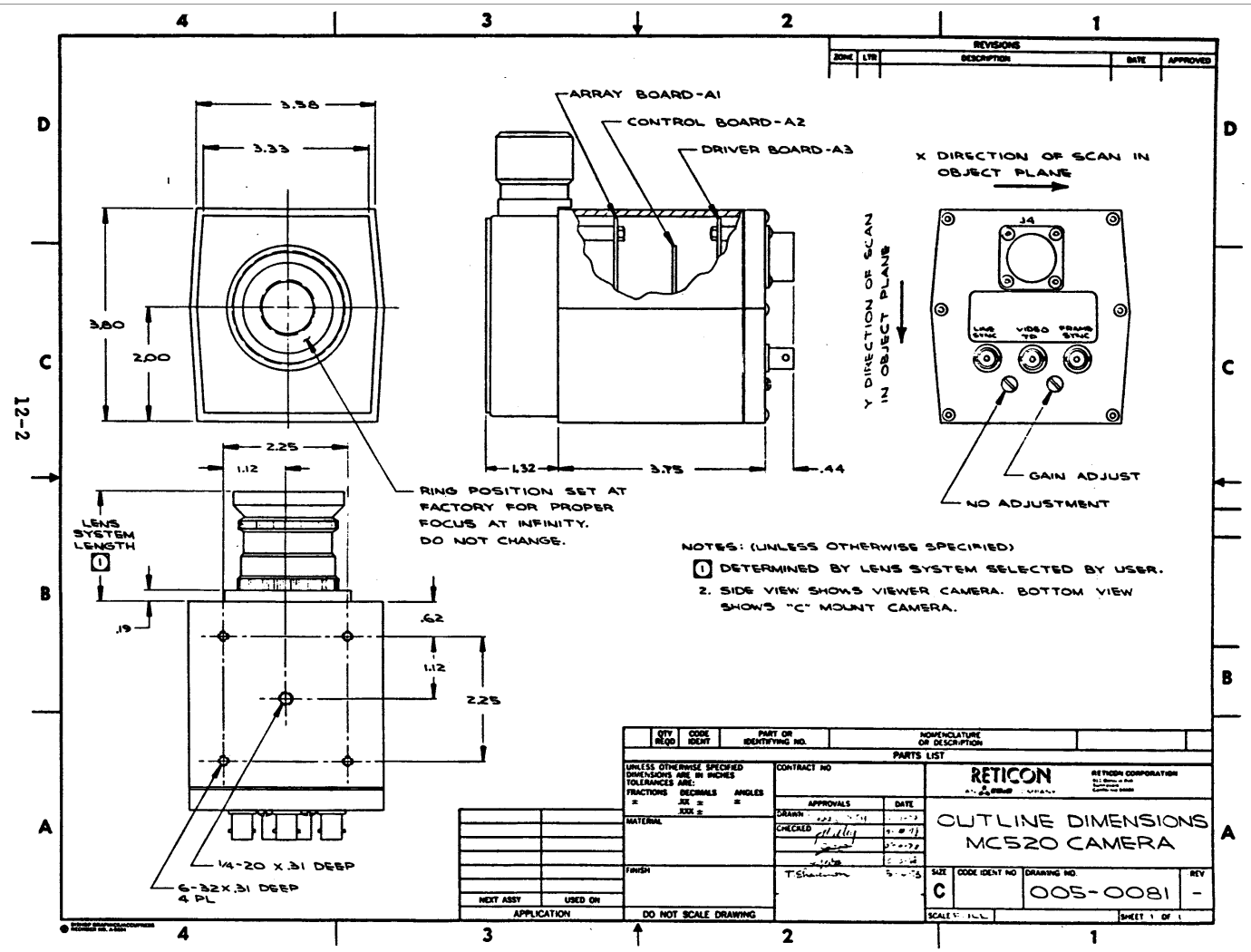
Retrace Count	S2 Settings 1	2	3	4
3	1	1	0	0
4	0	0	1	0
5	1	0	1	0
6	0	1	1	0
7	1	1	1	0
8	0	0	0	1
9	1	0	0	1
10	0	1	0	1
11	1	1	0	1
12	0	0	1	1
13	1	1	1	1
14	0	1	1	1
15	1	1	1	1
	1	2	4	8

Binary Weight



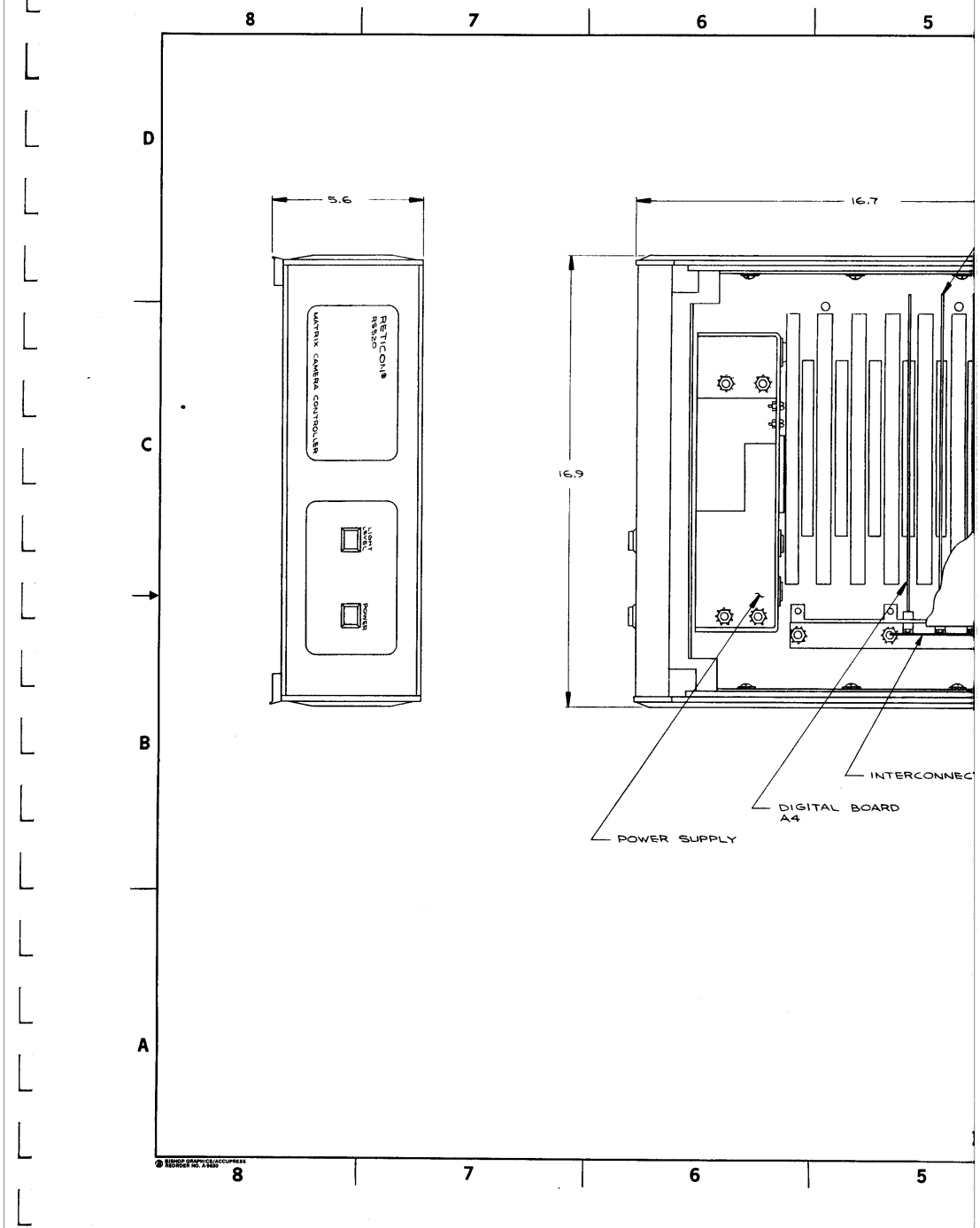
S2 - Front View

NOTES:
1. A "1" IN TABLE INDICATES SWITCH IS CLOSED, I.E., ROCKER IS DEPRESSED TOWARD NUMBERS PRINTED ON SWITCH BODY.
2. MINIMUM COUNT SETTING IS 2(FMHz +1), WHERE FMHz IS PIXEL RATE. FOR EXAMPLE, IF PIXEL RATE IS 1.7 MHz, MINIMUM COUNT WOULD BE 2(1.7 +1) = 5.4 -USE NEXT HIGHEST INTEGER = 6 & SET SWITCHES AS SHOWN IN TABLE FOR THAT COUNT.
3. TO CHANGE PIXEL RATE OVER MAXIMUM SPECIFIED RANGE OF .25-5 MHz WITHOUT CHANGING RETRACE COUNT, SET COUNT TO 12.
4. ACTUAL LINE RETRACE INTERVAL WILL BE (COUNT +2)T, WHERE T = PIXEL INTERVAL = $1/F_{MHz}$.

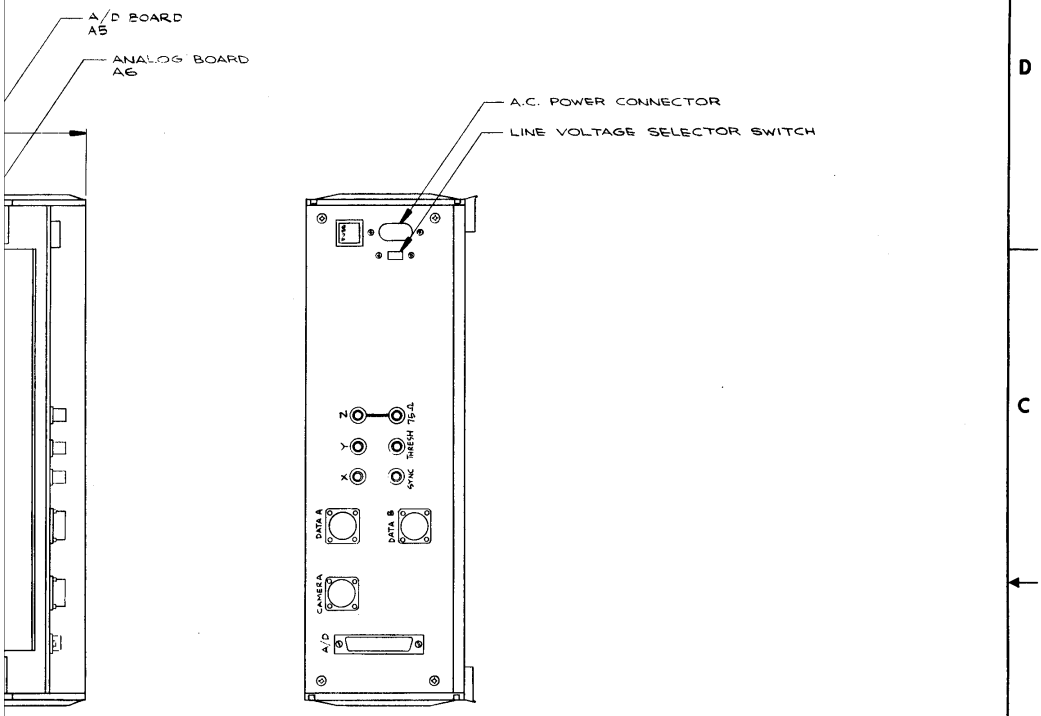

REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
3.58
3.33
3.80
2.00
2.25
1.12
LENS SYSTEM LENGTH
1
.19
.62
1.12
2.25
1/4-20 X .31 DEEP
6-32 X .31 DEEP 4 PL
RING POSITION SET AT FACTORY FOR PROPER FOCUS AT INFINITY. DO NOT CHANGE.
ARRAY BOARD-A1
CONTROL BOARD-A2
DRIVER BOARD-A3
1.32
3.75
.44
X DIRECTION OF SCAN IN OBJECT PLANE
Y DIRECTION OF SCAN IN OBJECT PLANE
J4
LINE SYNC
VIDEO TP
FRAME SYNC
GAIN ADJUST
NO ADJUSTMENT
NOTES: (UNLESS OTHERWISE SPECIFIED)
1 DETERMINED BY LENS SYSTEM SELECTED BY USER.
2. SIDE VIEW SHOWS VIEWER CAMERA. BOTTOM VIEW SHOWS "C" MOUNT CAMERA.
QTY REQD
CODE IDENT
PART OR IDENTIFYING NO.
NOMENCLATURE OR DESCRIPTION
PARTS LIST
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±
MATERIAL
FINISH
NEXT ASSY
USED ON
APPLICATION
DO NOT SCALE DRAWING
CONTRACT NO
APPROVALS
DATE
DRAWN
CHECKED
T Shannon
RETICON
RETICON CORPORATION
OUTLINE DIMENSIONS
MC520 CAMERA
SIZE C
CODE IDENT NO
DRAWING NO. 005-0081
REV -
SCALE
SHEET 1 OF 1
12-2

SECTION XII

LIST OF DRAWINGS


8
7
6
5
D
C
B
A
5.6
16.7
16.9
RETICON
MATRIX CAMERA CONTROLLER
LIGHT LEVEL
POWER
INTERCONNEC
DIGITAL BOARD
A4
POWER SUPPLY

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	INCORP ECO # 596	6-26-79	



RD

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN	5-11-78
CHECKED	5-10-78
	5-11-78
	5-10-78
T. Shuman	5-11-78

RETICON
AN EG&G COMPANY

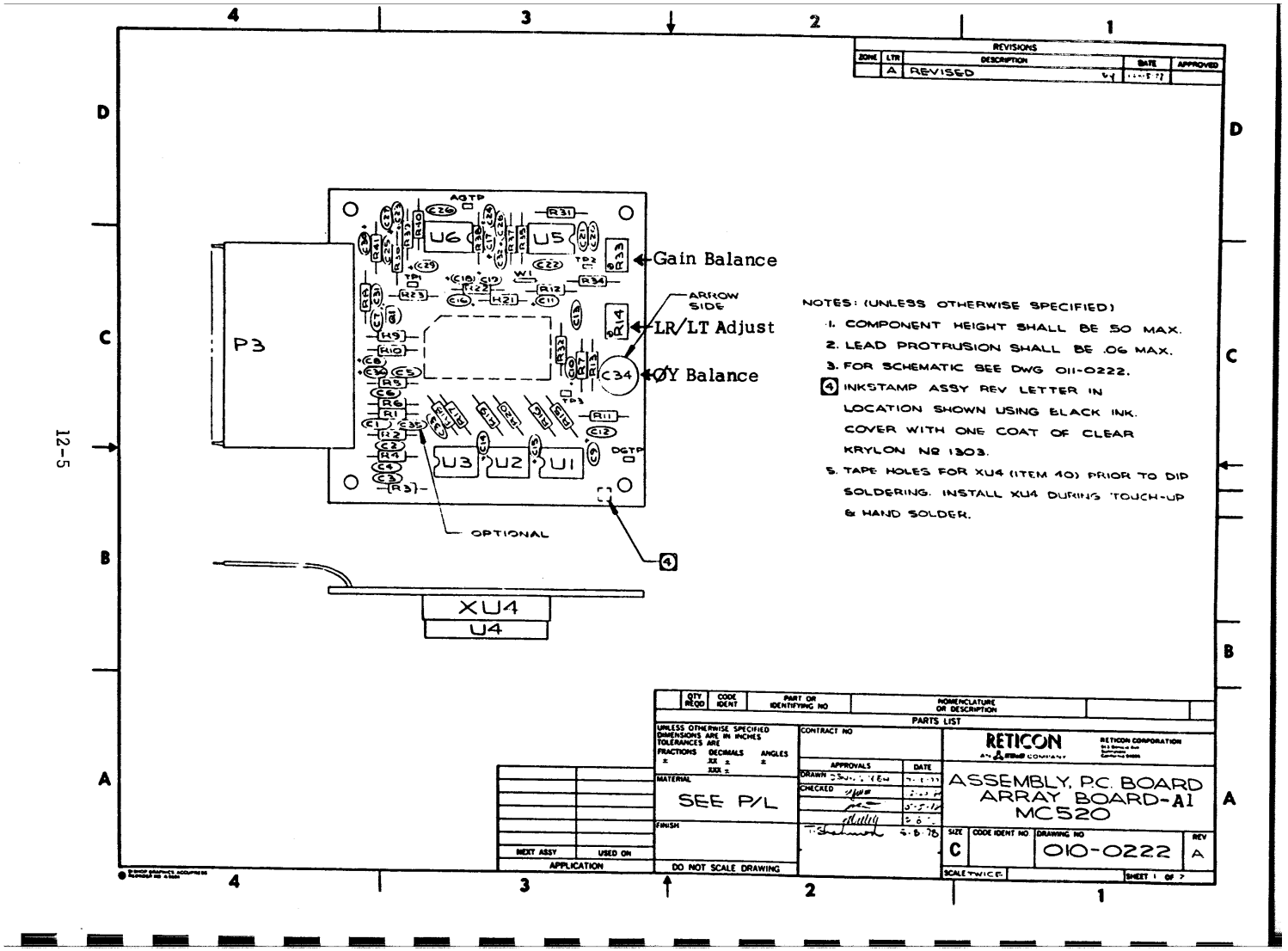
RETICON CORPORATION
910 Benecia Ave
Sunnyvale
California 94086

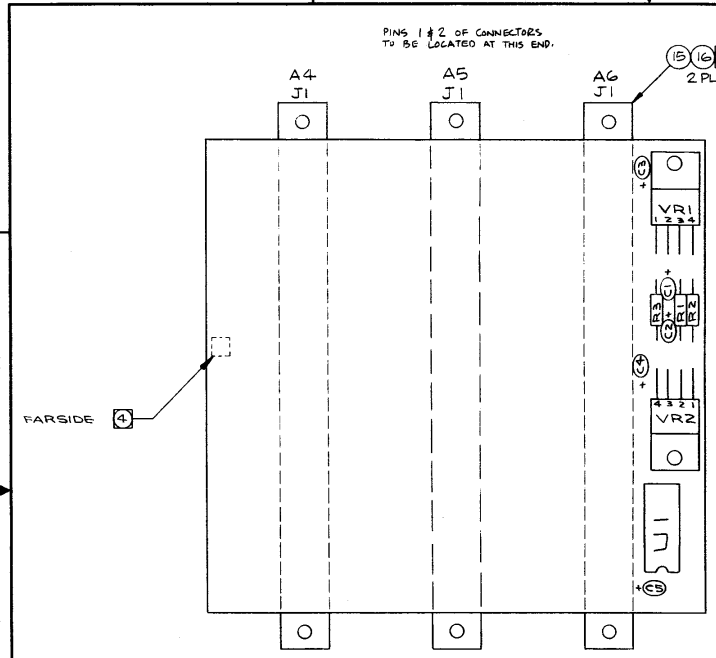
OUTLINE DIMENSIONS
RS520 CAMERA
CONTROLLER

SIZE	CODE IDENT NO.	DRAWING NO.	REV
D		005-0082	A

SCALE HALF SHEET 1 OF 1

NEXT ASSY	USED ON
APPLICATION	


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
A | REVISED
P3
Gain Balance
ARROW SIDE
LR/LT Adjust
ØY Balance
C34
OPTIONAL
XU4
U4
NOTES: (UNLESS OTHERWISE SPECIFIED)
1. COMPONENT HEIGHT SHALL BE .50 MAX.
2. LEAD PROTRUSION SHALL BE .06 MAX.
3. FOR SCHEMATIC SEE DWG 011-0222.
4 INKSTAMP ASSY REV LETTER IN LOCATION SHOWN USING BLACK INK. COVER WITH ONE COAT OF CLEAR KRYLON NO 1303.
5. TAPE HOLES FOR XU4 (ITEM 40) PRIOR TO DIP SOLDERING. INSTALL XU4 DURING TOUCH-UP & HAND SOLDER.
QTY REQD | CODE IDENT | PART OR IDENTIFYING NO | NOMENCLATURE OR DESCRIPTION
PARTS LIST
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±
MATERIAL SEE P/L
FINISH
NEXT ASSY | USED ON
APPLICATION
DO NOT SCALE DRAWING
CONTRACT NO
APPROVALS | DATE
DRAWN
CHECKED
RETICON
RETICON CORPORATION
ASSEMBLY, P.C. BOARD
ARRAY BOARD-A1
MC520
SIZE C | CODE IDENT NO | DRAWING NO 010-0222 | REV A
SCALE TWICE | SHEET 1 OF 2



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. COMPONENT HEIGHT SHALL BE .50 MAX.
2. LEAD PROTRUSION SHALL BE .06 MAX.
3. FOR SCHEMATIC SEE DWG 022-0063
4. INKSTAMP ASSY REV LETTER IN LOCATION SHOWN USING BLACK INK. COVER WITH ONE COAT OF CLEAR KRYLON N21303.
5. HOLES IN TABS OF VR1 & VR2 MUST LINE UP WITH HOLES IN PC BOARD PRIOR TO SOLDERING.
6. INSERT POLARIZING KEY, ITEM 16, INTO CONNECTORS AS FOLLOWS:
   - A4 J1 : BETWEEN PINS 24 & 26
   - A5 J1 : BETWEEN PINS 28 & 30
   - A6 J1 : BETWEEN PINS 32 & 34

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL: SEE P/L

FINISH

DO NOT SCALE DRAWING

APPROVALS	DATE
DRAWN T. Ehrnisch	4-26-79
CHECKED	

CONTRACT NO.

RETICON AN EG&G COMPANY
RETICON CORPORATION
910 Benicia Ave
Sunnyvale
California 94086

ASSEMBLY, P.C. BOARD
INTERCONNECT BOARD
RS520

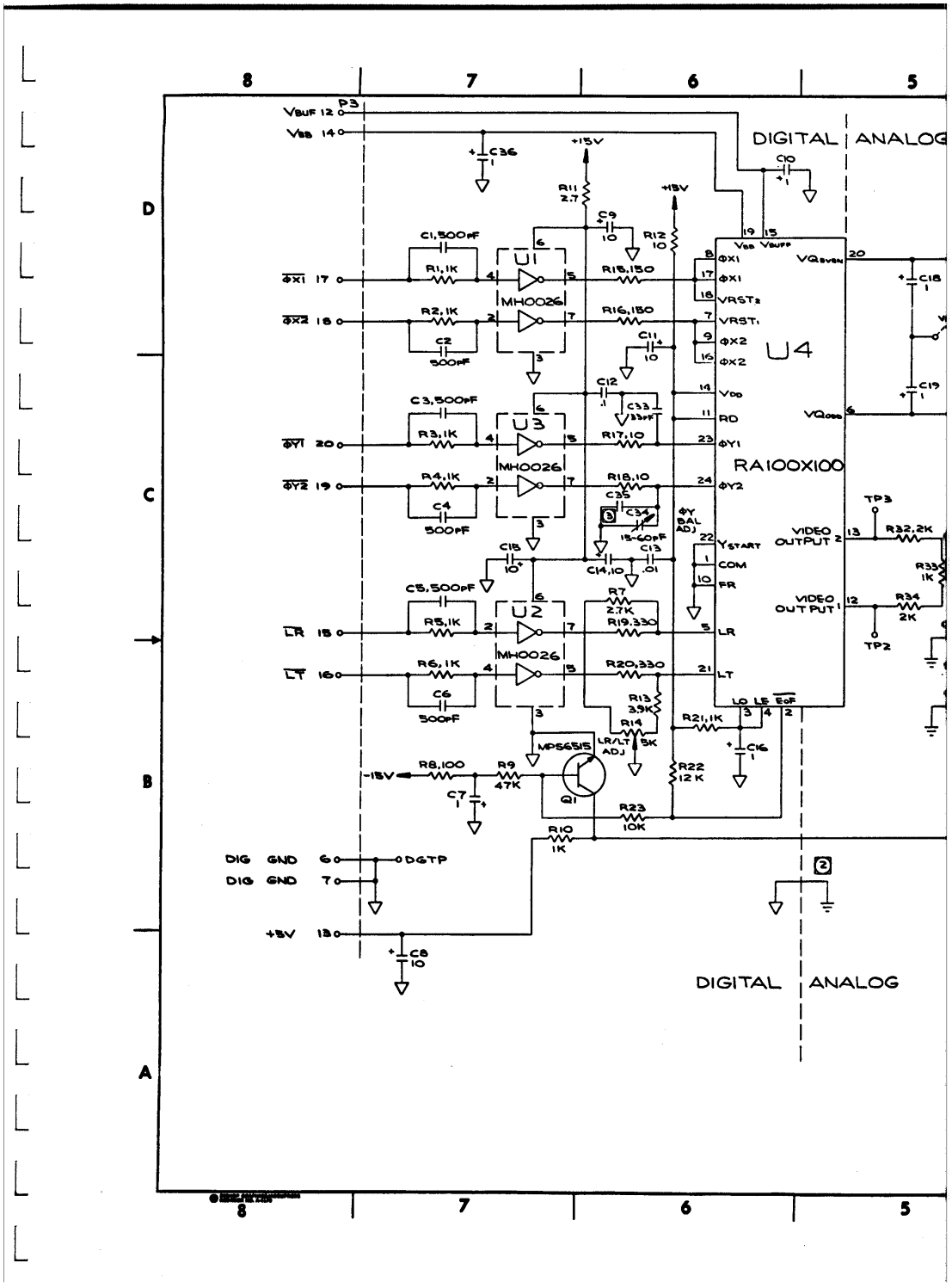
SIZE	CODE IDENT NO.	DRAWING NO.	REV
C		010-0323	-

SCALE TWICE | SHEET 1 OF 1

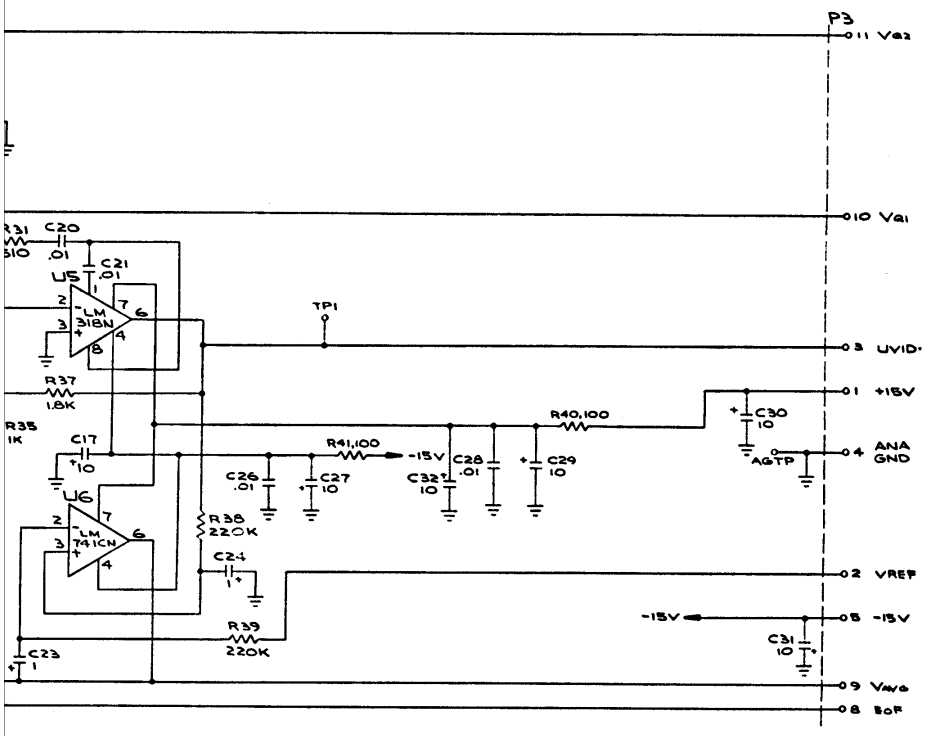
001-0266	RS520
NEXT ASSY	USED ON
APPLICATION	

BISHOP GRAPHICS/XEROX PRINTER NO. 4-9004

12-4


8
7
6
5
D
C
B
A
P3
VBUF 12
VSS 14
+15V
-15V
+5V
C36
C10
C9
C8
R11 2.7
R12 10
C1,500pF
R1,1K
C2 500pF
C3,500pF
R3,1K
C4 500pF
C5,500pF
R5,1K
C6 500pF
R6,1K
C12 .1
C33 33pF
C11 10
R15,150
R16,150
R17,10
R18,10
C35
C34 15-60pF
C14,10
C13 .01
C15 10
R7 2.7K
R19,330
R20,330
R13 39K
R14 5K
LR/LT ADJ
R21,1K
C16 1
R22 12K
R23 10K
R10 1K
R8,100
R9 47K
C7 1
MPS6515
Q1
U1
U2
U3
MH0026
U4
RA100X100
ΦX1
ΦX2
VRST1
VRST2
VDD
RD
ΦY1
ΦY2
ΦY BAL ADJ
YSTART
COM
FR
LR
LT
LO LE EOF
VQEVEN
VQODD
VIDEO OUTPUT 2
VIDEO OUTPUT 1
R32,2K
R33 1K
R34 2K
TP3
TP2
C18 1
C19 1
ΦX1 17
ΦX2 18
ΦY1 20
ΦY2 19
LR 15
LT 16
DIG GND 6
DIG GND 7
+5V 13
DGTP
DIGITAL
ANALOG
2

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	REVISED D.F.	11-13-77	



REF DESIGS	
HIGHEST USED	NOT USED
R41	R24-30
C36	
U6	
W1	
TP3	
Q1	
P3	P1,2
AGTP	
DOTP	

NOTES: (UNLESS OTHERWISE SPECIFIED)

1. RESISTORS ARE IN OHMS, ¼ W, 5%.
   CAPACITORS ARE IN MICROFARADS.
2. GROUND PLANES CONNECTED AT PIN 1 OF U4 ONLY.
3. OPTIONAL.
4. TP2,3 ARE NOT ON SERIAL NO 78039 TO 78045.

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN	
CHECKED	12-14-77
	5-1-78
T. Shemsky	5-8-78

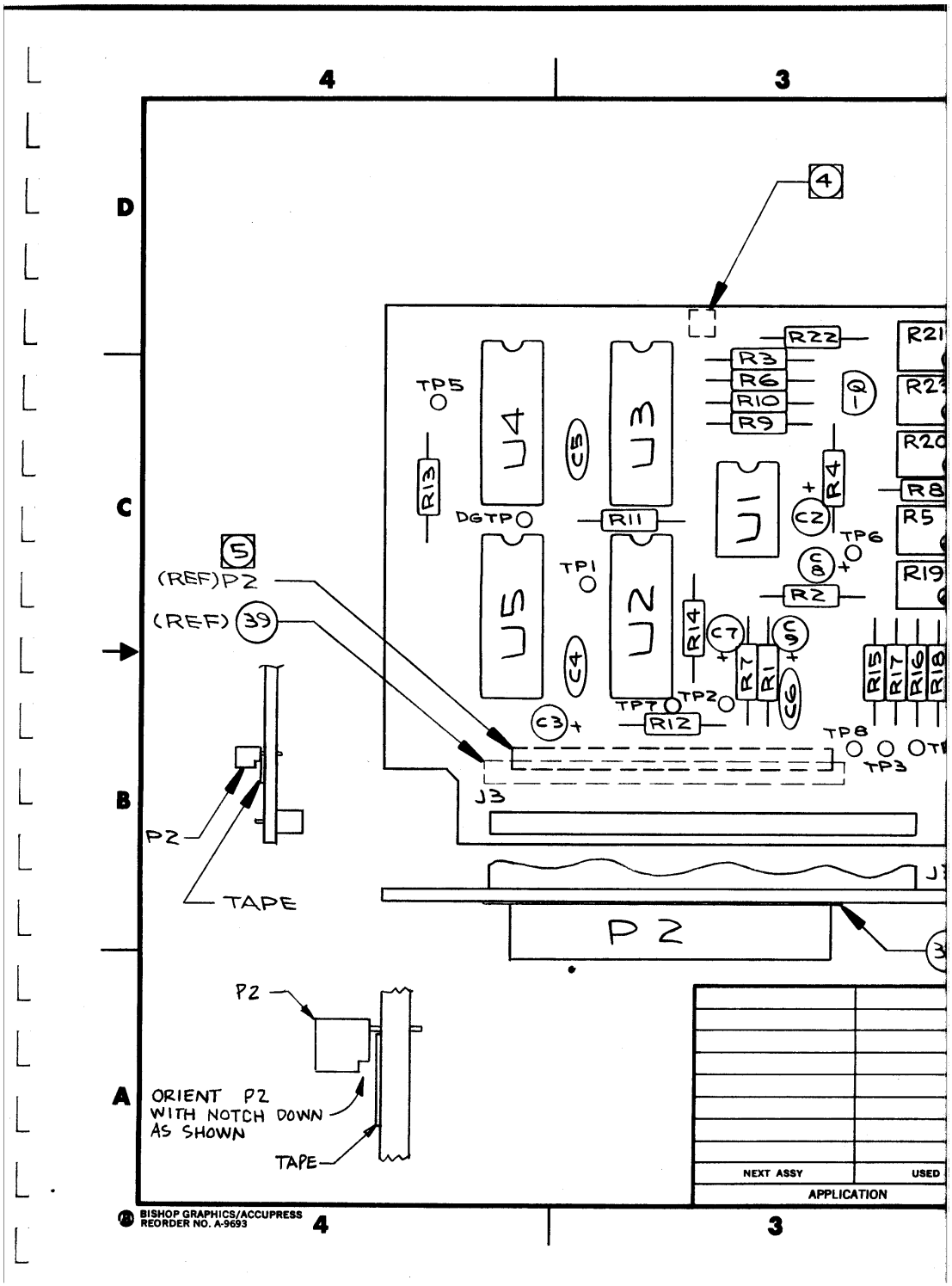
RETICON — RETICON CORPORATION, 910 Benecia Ave, Sunnyvale, California 94086

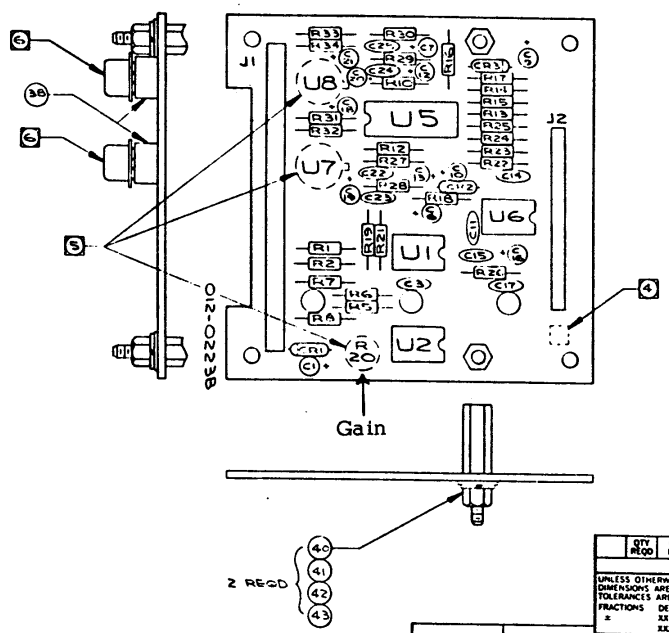
SCHEMATIC
ARRAY BOARD - A1
MC520

SIZE	CODE IDENT NO.	DRAWING NO.	REV
D		011-0222	A

SCALE NONE SHEET 1 OF 1

NEXT ASSY	USED ON
APPLICATION	


4
3
D
C
B
A
4
5
(REF) P2
(REF) 39
P2
TAPE
P2
ORIENT P2
WITH NOTCH DOWN
AS SHOWN
TAPE
J4
J3
J5
J2
J1
J3
P 2
TP5
DGTP
TP1
TP2
TP3
TP6
TP8
R13
R11
R12
R14
R22
R3
R6
R10
R9
R4
R2
R5
R19
R15
R17
R16
C5
C4
C3
C2
C8
C7
C6
Q1
NEXT ASSY
USED
APPLICATION
BISHOP GRAPHICS/ACCUPRESS
REORDER NO. A-9693



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. COMPONENT HEIGHT SHALL BE .50 MAX.
2. LEAD PROTRUSION SHALL BE .06 MAX.
3. FOR SCHEMATIC SEE DWG 011-0223.
4. INKSTAMP ACSY REV LETTER IN LOCATION SHOWN USING BLACK INK. COVER WITH ONE COAT OF CLEAR KRYLON NO 1303.
5. TAPE HOLES ON CIRCUIT SIDE OF BOARD FOR U8, U7 & R20 BEFORE SOLDERING. INSTALL U8, U7 & R20 ON CIRCUIT SIDE OF BOARD DURING TOUCH-UP & HAND SOLDER.
6. MUST BE MOUNTED CORRECTLY TO MATE WITH HEAT SINKS ON REAR PANEL.

REVISIONS

ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	REVISED		

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO	NOMENCLATURE OR DESCRIPTION
			PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE
FRACTIONS ± DECIMALS XX ± XXX ± ANGLES ±

MATERIAL: SEE P/L

FINISH:

NEXT ASSY | USED ON

APPLICATION

DO NOT SCALE DRAWING

CONTRACT NO

APPROVALS	DATE
DRAWN	
CHECKED	
	5-8-78
T. Chenault	5-8-78

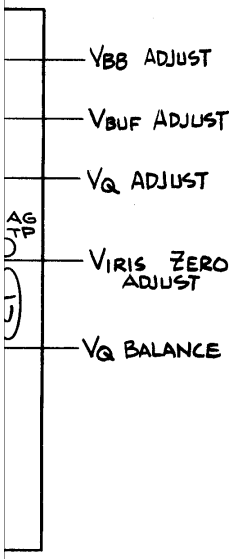
RETICON CORPORATION

ASSEMBLY, P.C. BOARD DRIVER BOARD MC520

SIZE	CODE IDENT NO	DRAWING NO	REV
C		010-0223	A

SCALE: NONE | SHEET 1 OF 2

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVAL
	A	REVISED D.Y.	12-15-77	
	B	INCORP ECO # 562	7-21-78	TAS
	C	INCORP ECO # 652	12-4-79	TAS

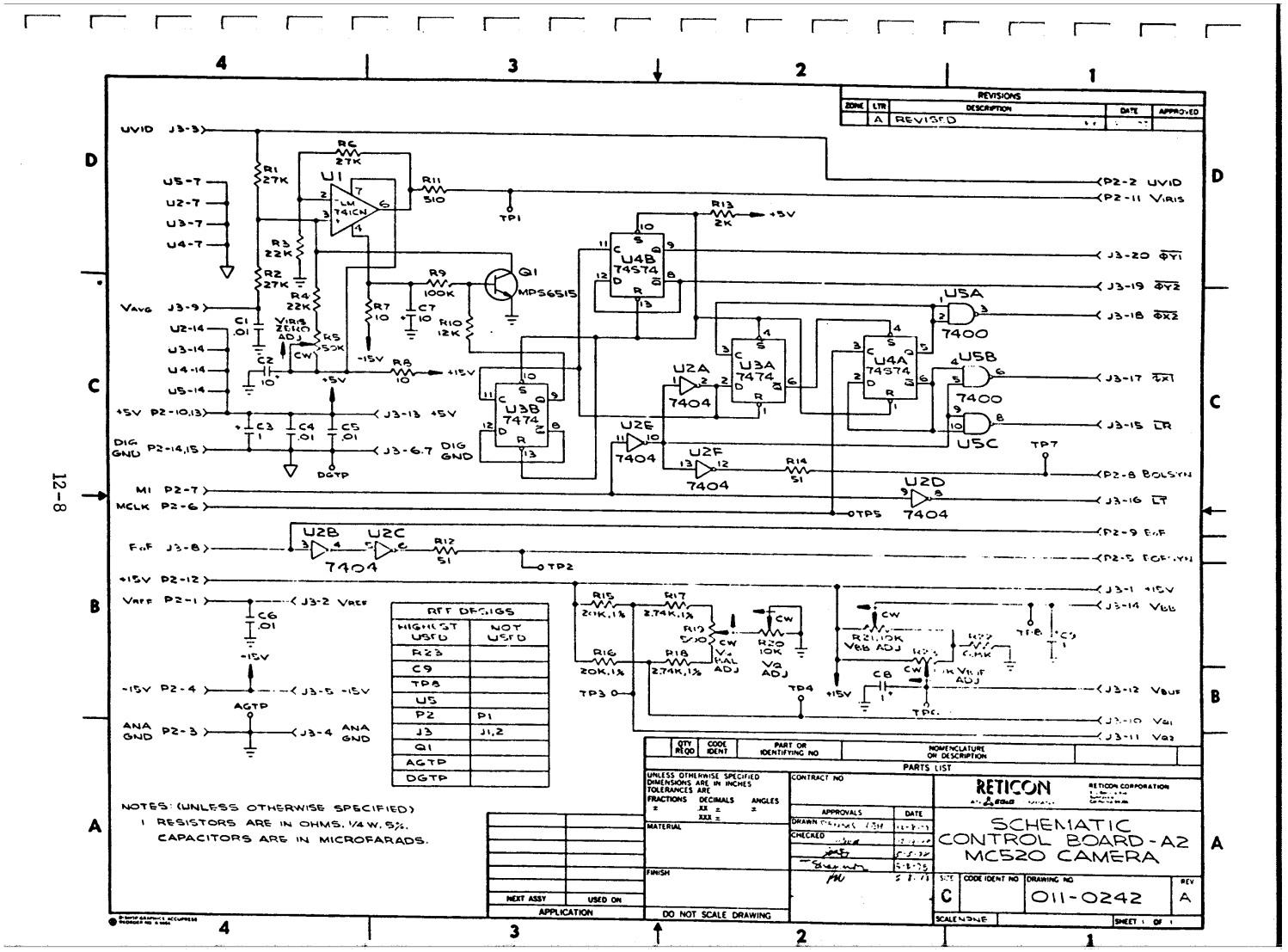


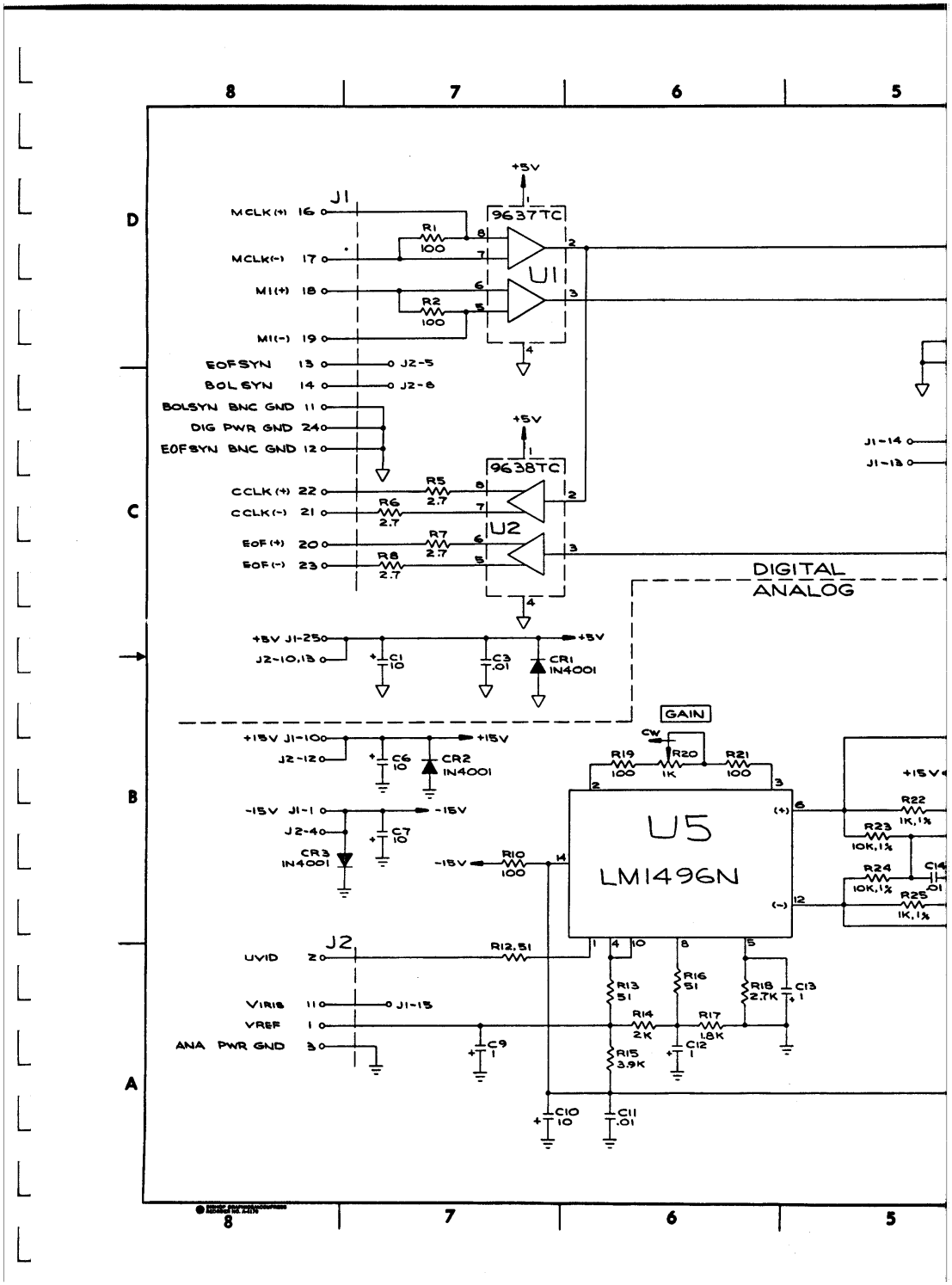
NOTES: (UNLESS OTHERWISE SPECIFIED)

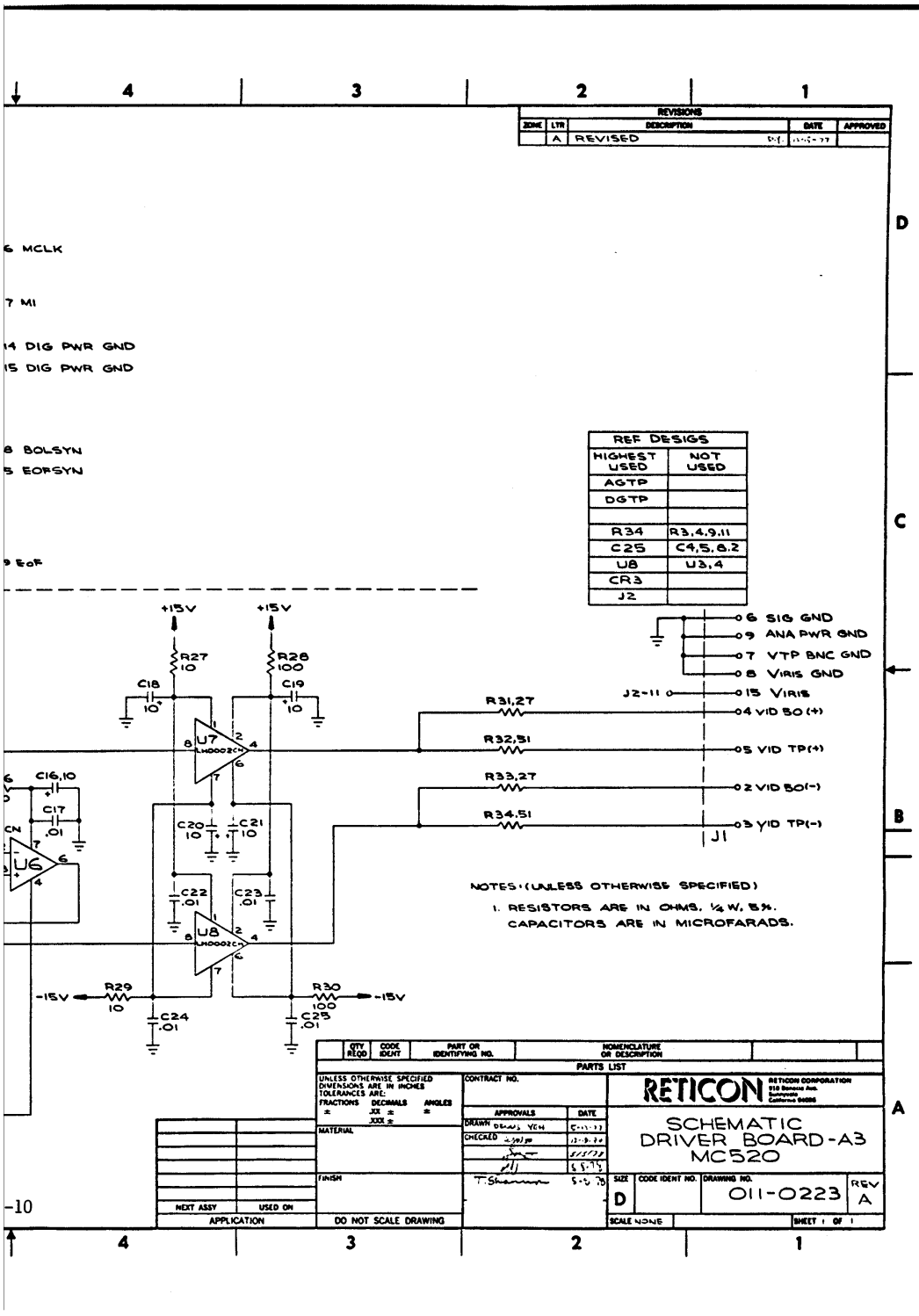
1. COMPONENT HEIGHT SHALL BE .50 MAX.
2. LEAD PROTRUSION SHALL BE .06 MAX.
3. FOR SCHEMATIC SEE DWG 011-0242.
4. INKSTAMP ASSY REV LETTER IN LOCATION SHOWN USING BLACK INK. COVER WITH ONE COAT OF CLEAR KRYLON Nº 1303.
5. TAPE HOLES FOR P2 PRIOR TO DIP SOLDERING. INSTALL P2 DURING TOUCH-UP & HAND SOLDER.

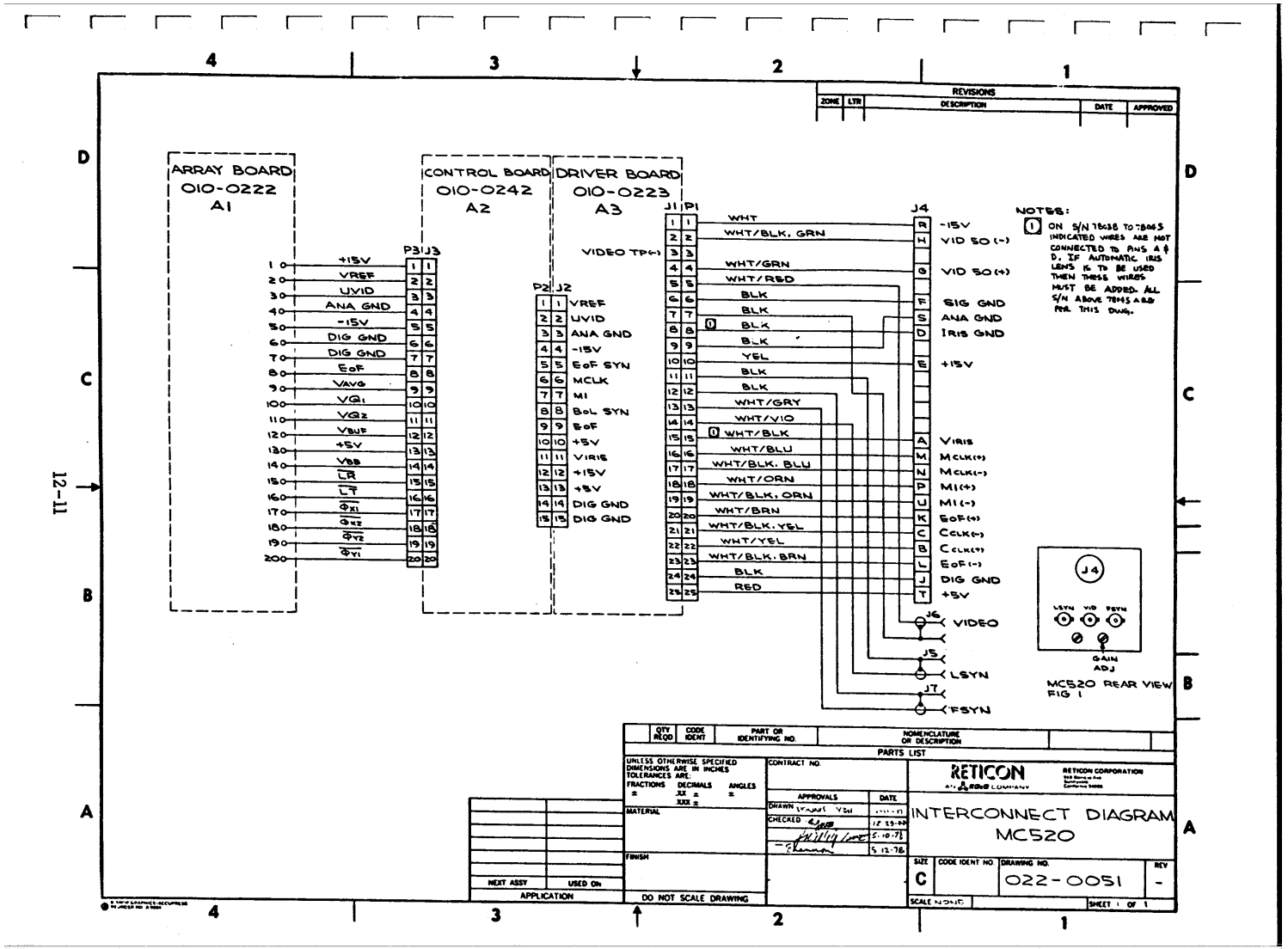
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS DECIMALS ANGLES ± .XX ± ± .XXX ±	CONTRACT NO.	RETICON AN EG&G COMPANY	RETICON CORPORATION 910 Benicia Ave. Sunnyvale California 94086
MATERIAL SEE P/L	APPROVALS / DRAWN D.Y.G.	12-12-77	ASSEMBLY, P.C. BOARD CONTROL BOARD-A2 MC520 CAMERA
FINISH	CHECKED	12-19-77	
DO NOT SCALE DRAWING		5-5-78	SIZE B / CODE IDENT NO. / DRAWING NO. 010-0242 / REV C
	T. Shannon	5.8.78 5-8-78	SCALE TWICE / SHEET 1 OF 2

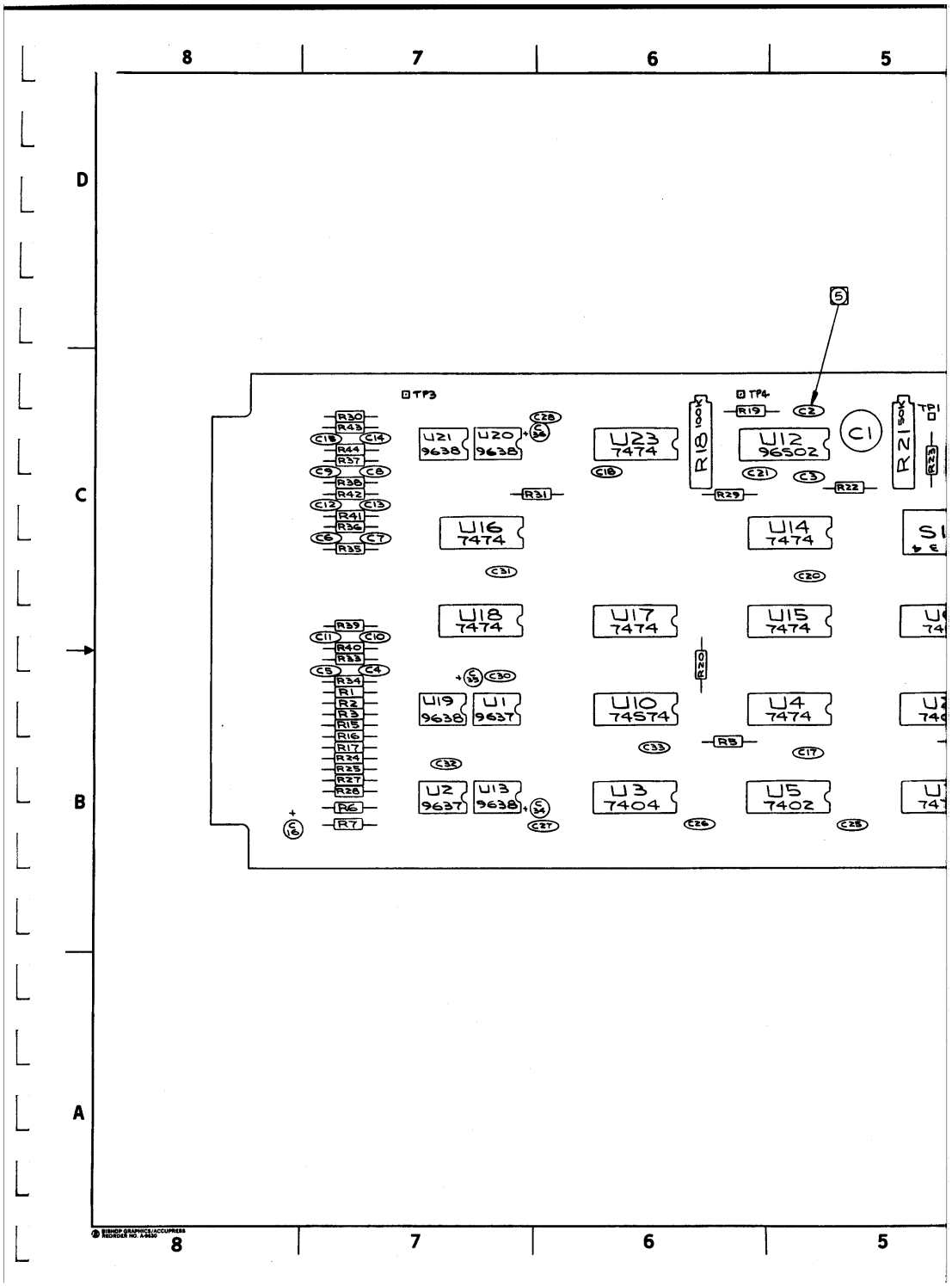
12-7


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
A | REVISED
NOTES: (UNLESS OTHERWISE SPECIFIED)
1 RESISTORS ARE IN OHMS, 1/4 W, 5%.
CAPACITORS ARE IN MICROFARADS.
REF DESIGS
HIGHEST USED | NOT USED
R23 |
C9 |
TP8 |
U5 |
P2 | P1
J3 | J1,2
Q1 |
AGTP |
DGTP |
PARTS LIST
QTY REQD | CODE IDENT | PART OR IDENTIFYING NO | NOMENCLATURE OR DESCRIPTION
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE
FRACTIONS ± | DECIMALS .XX ± .XXX ± | ANGLES ±
MATERIAL
FINISH
NEXT ASSY | USED ON
APPLICATION
DO NOT SCALE DRAWING
CONTRACT NO
APPROVALS | DATE
DRAWN
CHECKED
RETICON
RETICON CORPORATION
SCHEMATIC
CONTROL BOARD-A2
MC520 CAMERA
SIZE C | CODE IDENT NO | DRAWING NO 011-0242 | REV A
SCALE NONE | SHEET 1 OF 1
UVID J3-3
VAVG J3-9
+5V P2-10,13
DIG GND P2-14,15
MI P2-7
MCLK P2-6
F&F J3-8
+15V P2-12
VREF P2-1
-15V P2-4
ANA GND P2-3
P2-2 UVID
P2-11 VIRIS
J3-20 ΦY1
J3-19 ΦY2
J3-18 ΦX2
J3-17 ΦX1
J3-15 LR
P2-8 BOLSYN
J3-16 LT
P2-9 F&F
P2-5 FOFSYN
J3-1 +15V
J3-14 VBB
J3-12 VBUF
J3-10 VG1
J3-11 VG2
J3-13 +5V
J3-6,7 DIG GND
J3-2 VREF
J3-5 -15V
J3-4 ANA GND
U1 LM 741CN
Q1 MPS6515
U2A U2B U2C U2D U2E U2F 7404
U3A U3B 7474
U4A U4B 74S74
U5A U5B U5C 7400
R1 27K
R2 27K
R3 22K
R4 22K
R5 50K VIRIS ZERO ADJ
R6 27K
R7 10
R8 10
R9 100K
R10 12K
R11 510
R12 51
R13 2K +5V
R14 51
R15 20K,1%
R16 20K,1%
R17 2.74K,1%
R18 2.74K,1%
R19 500 CW VL FINAL ADJ
R20 10K VG ADJ
R21 10K VBB ADJ
R22 C.1MK
R23 1K VBUF ADJ
C1 .01
C2 10
C3 1
C4 .01
C5 .01
C6 .01
C7 10
C8 1
C9 1
TP1
TP2
TP3
TP4
TP5
TP6
TP7
TP8
TPC
AGTP
DGTP

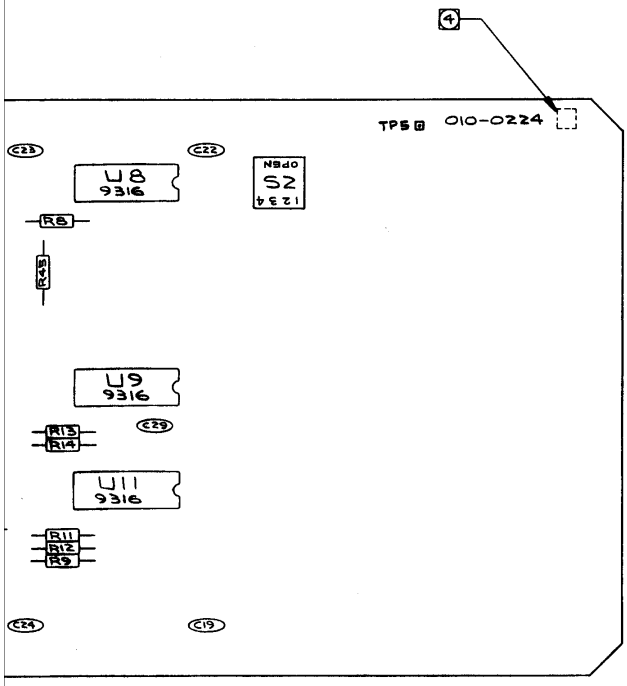

8
7
6
5
D
C
B
A
J1
MCLK(+) 16
MCLK(-) 17
MI(+) 18
MI(-) 19
EOFSYN 13
BOLSYN 14
BOLSYN BNC GND 11
DIG PWR GND 24
EOFSYN BNC GND 12
CCLK(+) 22
CCLK(-) 21
EOF(+) 20
EOF(-) 23
J2-5
J2-6
+5V
9637TC
U1
9638TC
U2
R1 100
R2 100
R5 2.7
R6 2.7
R7 2.7
R8 2.7
DIGITAL
ANALOG
+5V J1-25
J2-10,13
C1 10
C3 .01
CR1 IN4001
+15V J1-10
J2-12
C6 10
CR2 IN4001
-15V J1-1
J2-40
C7 10
CR3 IN4001
GAIN
CW
R19 100
R20 1K
R21 100
U5
LM1496N
R10 100
R22 1K,1%
R23 10K,1%
R24 10K,1%
R25 1K,1%
J2
UVID 2
VIRIB 11
VREF 1
ANA PWR GND 3
J1-15
R12,51
R13 51
R16 51
R18 2.7K
C13 1
R14 2K
R17 1.8K
R15 3.9K
C9 1
C12 1
C10 10
C11 .01


REVISIONS
ZONE LTR DESCRIPTION DATE APPROVED
A REVISED
6 MCLK
7 MI
14 DIG PWR GND
15 DIG PWR GND
8 BOLSYN
5 EOPSYN
9 EOF
REF DESIGS
HIGHEST USED
NOT USED
AGTP
DGTP
R34
R3,4,9,11
C25
C4,5,8,2
U8
U3,4
CR3
J2
+15V
+15V
R27 10
R28 100
C18 10
C19 10
U7
U8
C16,10
C17 .01
C20 10
C21 10
C22 .01
C23 .01
C24 .01
C23 .01
R29 10
R30 100
-15V
-15V
R31,27
R32,51
R33,27
R34,51
J2-11
6 SIG GND
9 ANA PWR GND
7 VTP BNC GND
8 VIRIS GND
15 VIRIS
4 VID SO (+)
5 VID TP(+)
2 VID SO(-)
3 VID TP(-)
J1
NOTES: (UNLESS OTHERWISE SPECIFIED)
1. RESISTORS ARE IN OHMS, ¼ W, 5%.
CAPACITORS ARE IN MICROFARADS.
QTY REQD
CODE IDENT
PART OR IDENTIFYING NO.
NOMENCLATURE OR DESCRIPTION
PARTS LIST
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
± .XX ± ±
.XXX ±
MATERIAL
FINISH
NEXT ASSY
USED ON
APPLICATION
DO NOT SCALE DRAWING
CONTRACT NO.
APPROVALS
DATE
DRAWN
CHECKED
T. Sherman
RETICON
RETICON CORPORATION
SCHEMATIC
DRIVER BOARD-A3
MC520
SIZE
D
CODE IDENT NO.
DRAWING NO.
011-0223
REV
A
SCALE NONE
SHEET 1 OF 1


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
ARRAY BOARD
010-0222
A1
CONTROL BOARD
010-0242
A2
DRIVER BOARD
010-0223
A3
P3 J3
P2 J2
J1 P1
J4
+15V
VREF
UVID
ANA GND
-15V
DIG GND
DIG GND
EOF
VAVG
VQ1
VQ2
VBUF
+5V
VBB
LR
LT
ΦX1
ΦX2
ΦY2
ΦY1
VREF
UVID
ANA GND
-15V
EOF SYN
MCLK
MI
BOL SYN
EOF
+5V
VIRIS
+15V
+5V
DIG GND
DIG GND
VIDEO TP(-)
WHT
WHT/BLK. GRN
WHT/GRN
WHT/RED
BLK
BLK
BLK
BLK
YEL
BLK
BLK
WHT/GRY
WHT/VIO
WHT/BLK
WHT/BLU
WHT/BLK. BLU
WHT/ORN
WHT/BLK. ORN
WHT/BRN
WHT/BLK. YEL
WHT/YEL
WHT/BLK. BRN
BLK
RED
-15V
VID SO (-)
VID SO (+)
SIG GND
ANA GND
IRIS GND
+15V
VIRIS
MCLK(+)
MCLK(-)
MI(+)
MI(-)
EOF(+)
CCLK(-)
CCLK(+)
EOF(-)
DIG GND
+5V
J6 VIDEO
J5 LSYN
J7 FSYN
NOTES:
1. ON S/N 78038 TO 78045 INDICATED WIRES ARE NOT CONNECTED TO PINS A & D. IF AUTOMATIC IRIS LENS IS TO BE USED THEN THESE WIRES MUST BE ADDED. ALL S/N ABOVE 78045 ARE PER THIS DWG.
J4
LSYN VID FSYN
GAIN ADJ
MC520 REAR VIEW
FIG 1
QTY REQD | CODE IDENT | PART OR IDENTIFYING NO. | NOMENCLATURE OR DESCRIPTION
PARTS LIST
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±
MATERIAL
FINISH
NEXT ASSY | USED ON
APPLICATION
DO NOT SCALE DRAWING
CONTRACT NO.
APPROVALS | DATE
DRAWN
CHECKED
12-23-77
5-10-78
5-12-78
RETICON
RETICON CORPORATION
INTERCONNECT DIAGRAM
MC520
SIZE C | CODE IDENT NO. | DRAWING NO. 022-0051 | REV -
SCALE NONE | SHEET 1 OF 1


8
7
6
5
D
C
B
A
TP3
TP4
U21 9638
U20 9638
U23 7474
U12 96502
U16 7474
U14 7474
U18 7474
U17 7474
U15 7474
U19 9638
U1 9637
U10 74S74
U4 7474
U2 9637
U13 9638
U3 7404
U5 7402
R18 100K
R21 50K
R20
R5
C1
C2
C3
C17
C18
C20
C21
C25
C26
C27
C28
C29
C30
C31
C32
C33
C34
C35
C36
R1
R2
R3
R5
R6
R7
R15
R16
R17
R19
R20
R22
R23
R24
R25
R26
R27
R28
R29
R30
R31
R34
R35
R36
R37
R38
R39
R40
R41
R42
R43
R44
C4
C5
C6
C7
C8
C9
C10
C11
C12
C13
C14
C15
C16
5

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	ADDED TP3, 4 & 5	10-16-78	
	B	INCORP ECO # 618	9-7-79	



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. COMPONENT HEIGHT SHALL BE .50 MAX.
2. LEAD PROTRUSION SHALL BE .06 MAX. EXCEPT FOR DIL LEADS.
3. FOR SCHEMATIC SEE DWG 011-0224.
4. INKSTAMP ASSY REV LETTER IN LOCATION SHOWN USING BLACK INK. COVER WITH ONE COAT OF CLEAR KRYLON N21303.
5. CAPACITOR C2 IS FACTORY SELECT.
6. CAPACITORS C4 – C15 ARE OPTIONAL DEPENDING ON USER'S CABLE LENGTH.

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION

PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL: SEE P/L

FINISH:

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN O. Ennis YSH	1-19-78
CHECKED T. Sherman	5-2-78
	5-9-78
	5-10-78

RETICON
AN EG&G COMPANY
RETICON CORPORATION
910 Benicia Ave.
Sunnyvale
California 94086

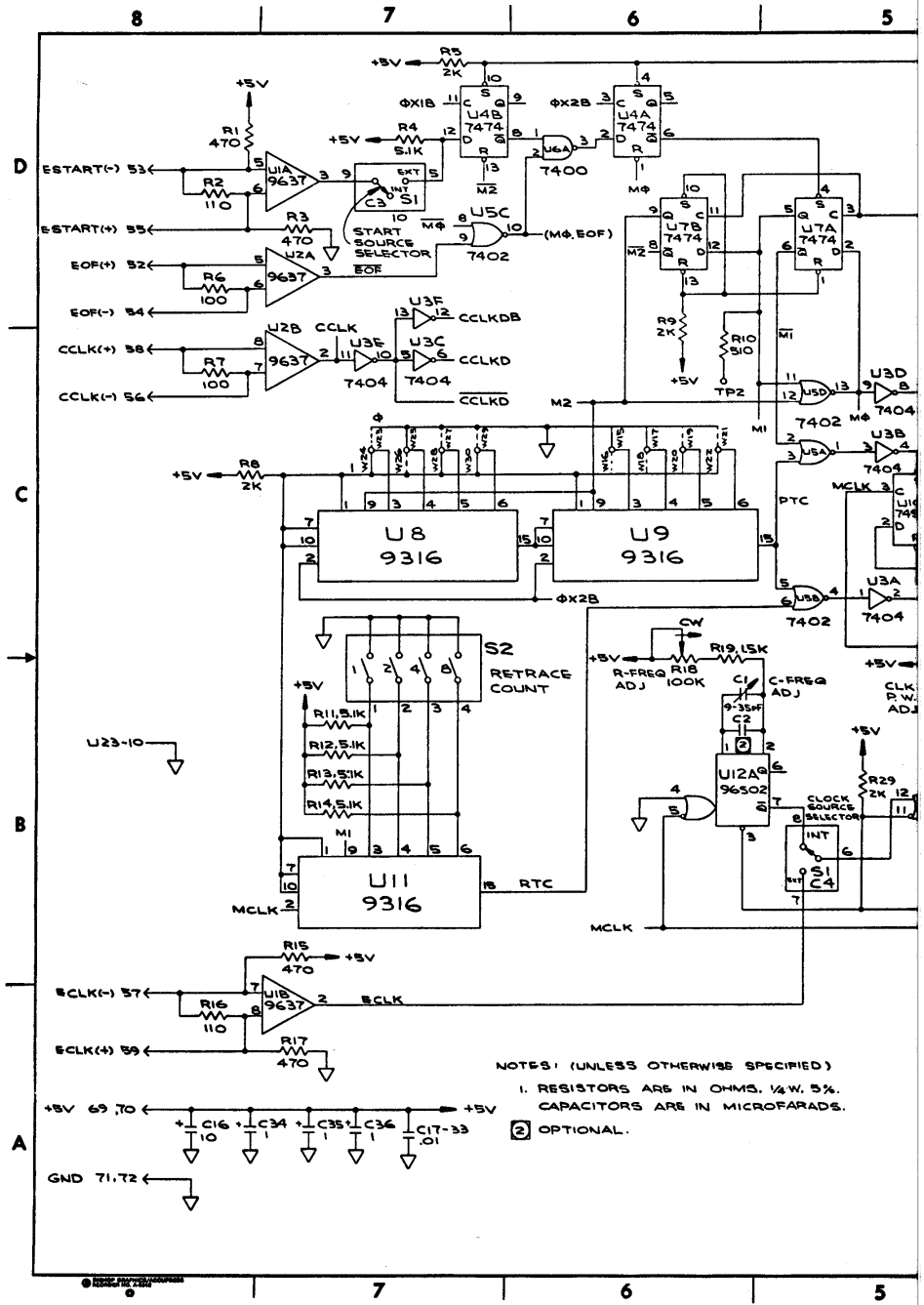
ASSEMBLY, P.C. BOARD
DIGITAL BOARD
RS 520

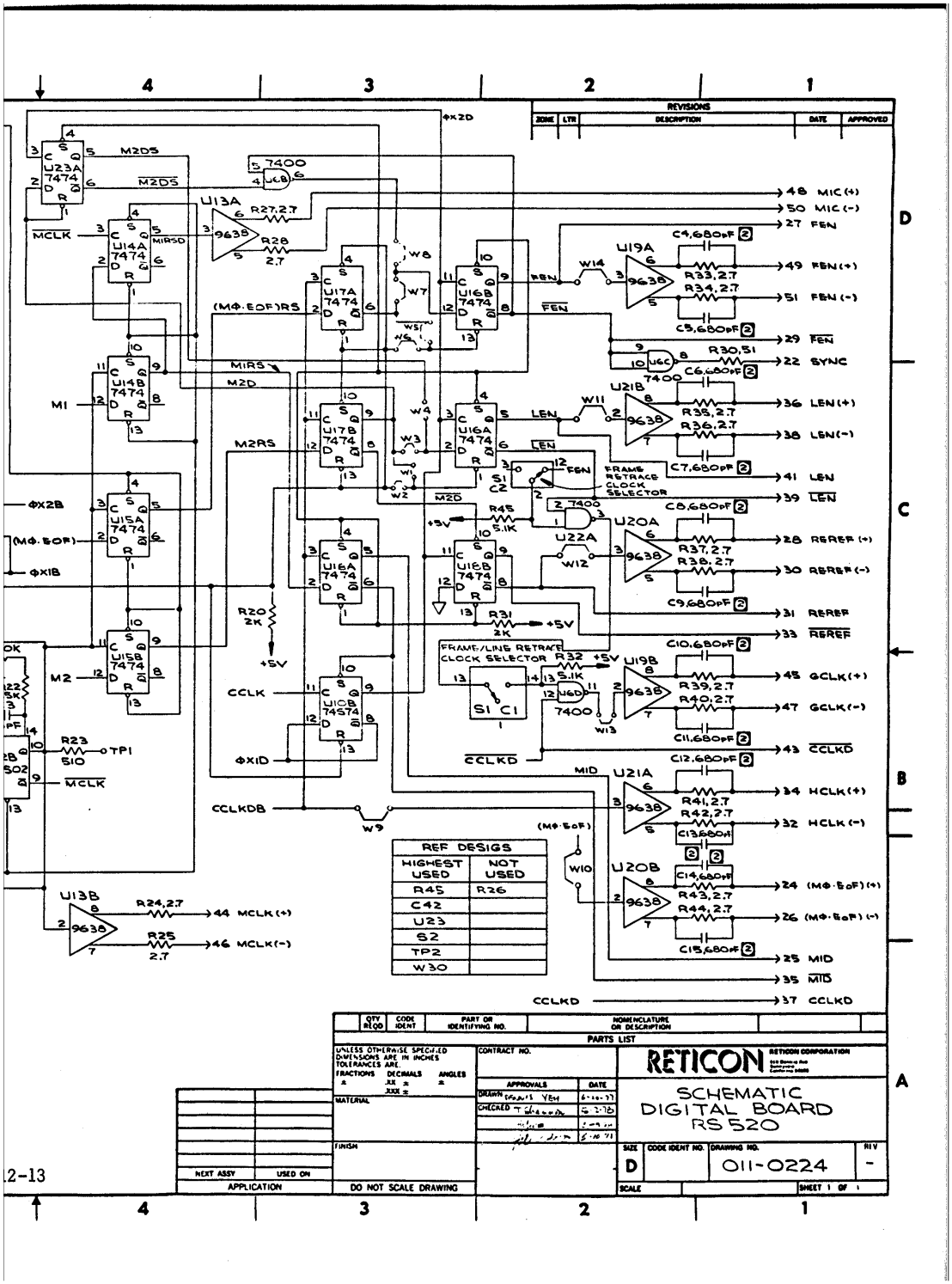
SIZE	CODE IDENT NO.	DRAWING NO.	REV
D		010-0224	B

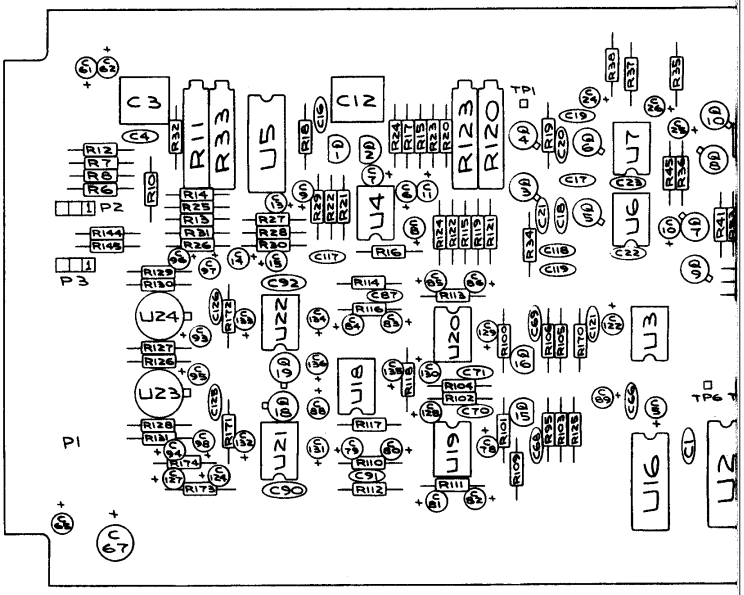
SCALE NONE SHEET 1 OF 1

NEXT ASSY	USED ON
APPLICATION	

12-12


8
7
6
5
D
C
B
A
+5V
R1 470
R2 110
R3 470
R4 5.1K
R5 2K
R6 100
R7 100
R8 2K
R9 2K
R10 510
R11 5.1K
R12 5.1K
R13 5.1K
R14 5.1K
R15 470
R16 110
R17 470
R18 100K
R19 1.5K
R29 2K
ESTART(-) 53
ESTART(+) 55
EOF(+) 52
EOF(-) 54
CCLK(+) 58
CCLK(-) 56
ECLK(-) 57
ECLK(+) 59
+5V 69,70
GND 71,72
U1A 9637
U2A 9637
U2B 9637
U1B 9637
U4B 7474
U4A 7474
U7B 7474
U7A 7474
U5C 7402
U5D 7402
U5A 7402
U5B 7402
U3F 7404
U3E 7404
U3C 7404
U3D 7404
U3B 7404
U3A 7404
U6A 7400
U8 9316
U9 9316
U11 9316
U12A 96502
S1 START SOURCE SELECTOR
S2 RETRACE COUNT
S1 CLOCK SOURCE SELECTOR
R-FREQ ADJ
C-FREQ ADJ
CW
9-35pF
C16 10
C34 1
C35 1
C36 1
C17-33 .01
ΦX1B
ΦX2B
M1
M2
MΦ
(MΦ,EOF)
CCLK
CCLKDB
CCLKD
PTC
RTC
MCLK
U23-10
TP2
INT
EXT
NOTES: (UNLESS OTHERWISE SPECIFIED)
1. RESISTORS ARE IN OHMS, 1/4W, 5%.
CAPACITORS ARE IN MICROFARADS.
2 OPTIONAL.

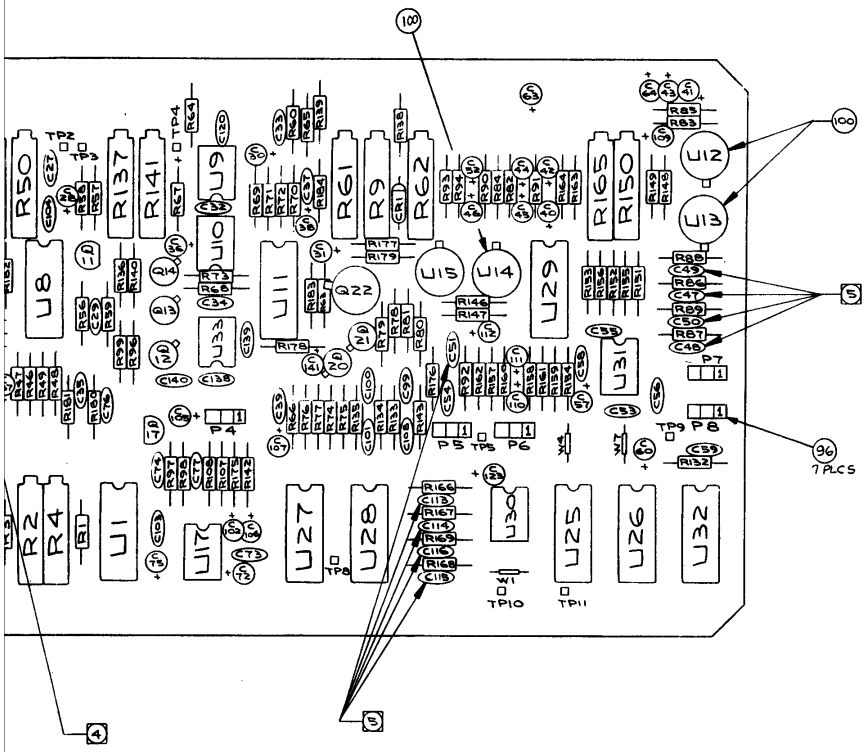

REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
4 3 2 1
D C B A
ΦX2D
M2DS
MCLK
MIRSD
U13A 9638 R27,2.7 R28 2.7
U14A 7474
U14B 7474
U15A 7474
U15B 7474
U16A 7474
U16B 7474
U17A 7474
U17B 7474
U18A 7474
U18B 7474
U19A 9638 R33,2.7 R34,2.7 C4,680pF C5,680pF
U19B 9638 R39,2.7 R40,2.7 C10,680pF C11,680pF
U20A 9638 R37,2.7 R38,2.7 C8,680pF C9,680pF
U20B 9638 R43,2.7 R44,2.7 C14,680pF C15,680pF
U21A 9638 R41,2.7 R42,2.7 C13,680pF
U21B 9638 R35,2.7 R36,2.7 C7,680pF
U13B 9638 R24,2.7 R25 2.7
U22A 7400
U6B 7400
U6C 7400
U6D 7400
R30,51 C6,680pF
R45 5.1K
R20 2K
R31 2K
R32 5.1K
R23 510
W1 W2 W3 W4 W5 W6 W7 W8 W9 W10 W11 W12 W13 W14
S1 C1 S2 C2
FRAME RETRACE CLOCK SELECTOR
FRAME/LINE RETRACE CLOCK SELECTOR
TP1
48 MIC(+)
50 MIC(-)
27 FEN
49 FEN(+)
51 FEN(-)
29 FEN
22 SYNC
36 LEN(+)
38 LEN(-)
41 LEN
39 LEN
28 REREF(+)
30 REREF(-)
31 REREF
33 REREF
45 GCLK(+)
47 GCLK(-)
43 CCLKD
34 HCLK(+)
32 HCLK(-)
24 (MΦ·EOF)(+)
26 (MΦ·EOF)(-)
25 MID
35 MID
37 CCLKD
44 MCLK(+)
46 MCLK(-)
REF DESIGS
HIGHEST USED | NOT USED
R45 | R26
C42 |
U23 |
S2 |
TP2 |
W30
QTY REQD | CODE IDENT | PART OR IDENTIFYING NO. | NOMENCLATURE OR DESCRIPTION
PARTS LIST
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE: FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±
MATERIAL
FINISH
NEXT ASSY | USED ON
APPLICATION
DO NOT SCALE DRAWING
CONTRACT NO.
APPROVALS | DATE
DRAWN | CHECKED
RETICON CORPORATION
SCHEMATIC DIGITAL BOARD RS520
SIZE D | CODE IDENT NO. | DRAWING NO. 011-0224 | REV -
SCALE | SHEET 1 OF 1
2-13



NOTES: (UNLESS OTHERWISE SPECIFIED)

1. COMPONENT HEIGHT SHALL BE .50 MAX.
2. LEAD PROTRUSION SHALL BE .09 MAX.
3. FOR SCHEMATIC SEE DWG 011-0225.
4. INKSTAMP ASSY REV LETTER IN LOCATION SHOWN USING BLACK INK COVER WITH ONE COAT OF CLEAR KRYLON #1303.
5. C47,48,49,50,51,113,114,115 & 116 ARE OPTIONAL DEPENDING ON USER'S CABLE LENGTH. DO NOT LOAD. KEEP HOLES FREE OF SOLDER.
6. DONOT REMOVE CONDUCTIVE RUBBER RING ON SD210 DEVICES UNTIL BOARD IS READY TO BE PLACED IN ANTI-STATIC BAG PRIOR TO TEST. BOARDS CONTAINING SD210 DEVICES MUST BE IN ANTI-STATIC BAG BETWEEN ALL TEST OPERATIONS AFTER THE RING IS REMOVED.

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	INCORP ECO# 395	4-20-79	



QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION
			PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL: SEE P/L

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN Dennis Yeh	1-10-78
CHECKED T. Swanson	5-8-78
[illegible]	5-10-78
[illegible]	5-11-78

RETICON
AN EG&G COMPANY
RETICON CORPORATION
910 Benicia Ave
Sunnyvale
California 94086

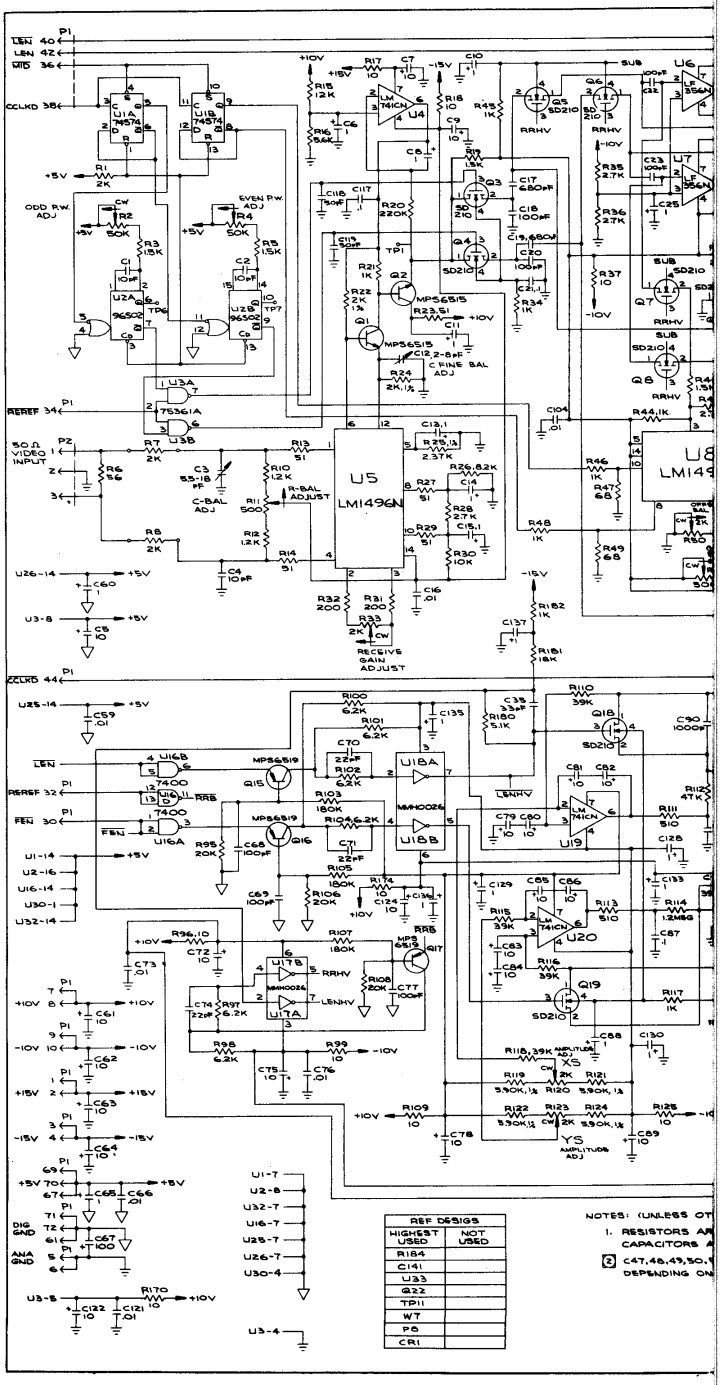
ASSEMBLY, P.C. BOARD
ANALOG BOARD
MC-520

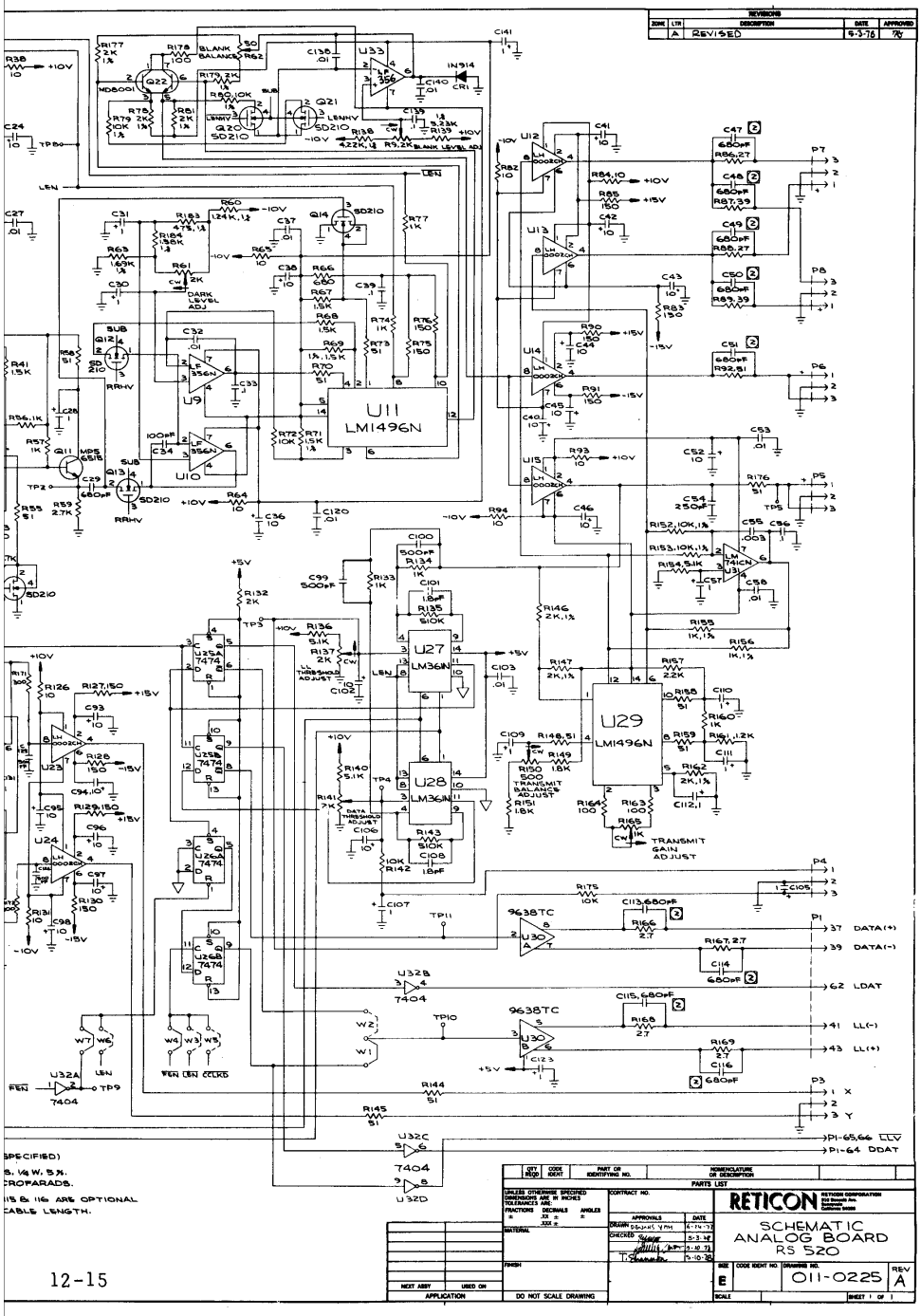
SIZE	CODE IDENT NO.	DRAWING NO.	REV
D		010-0225	A

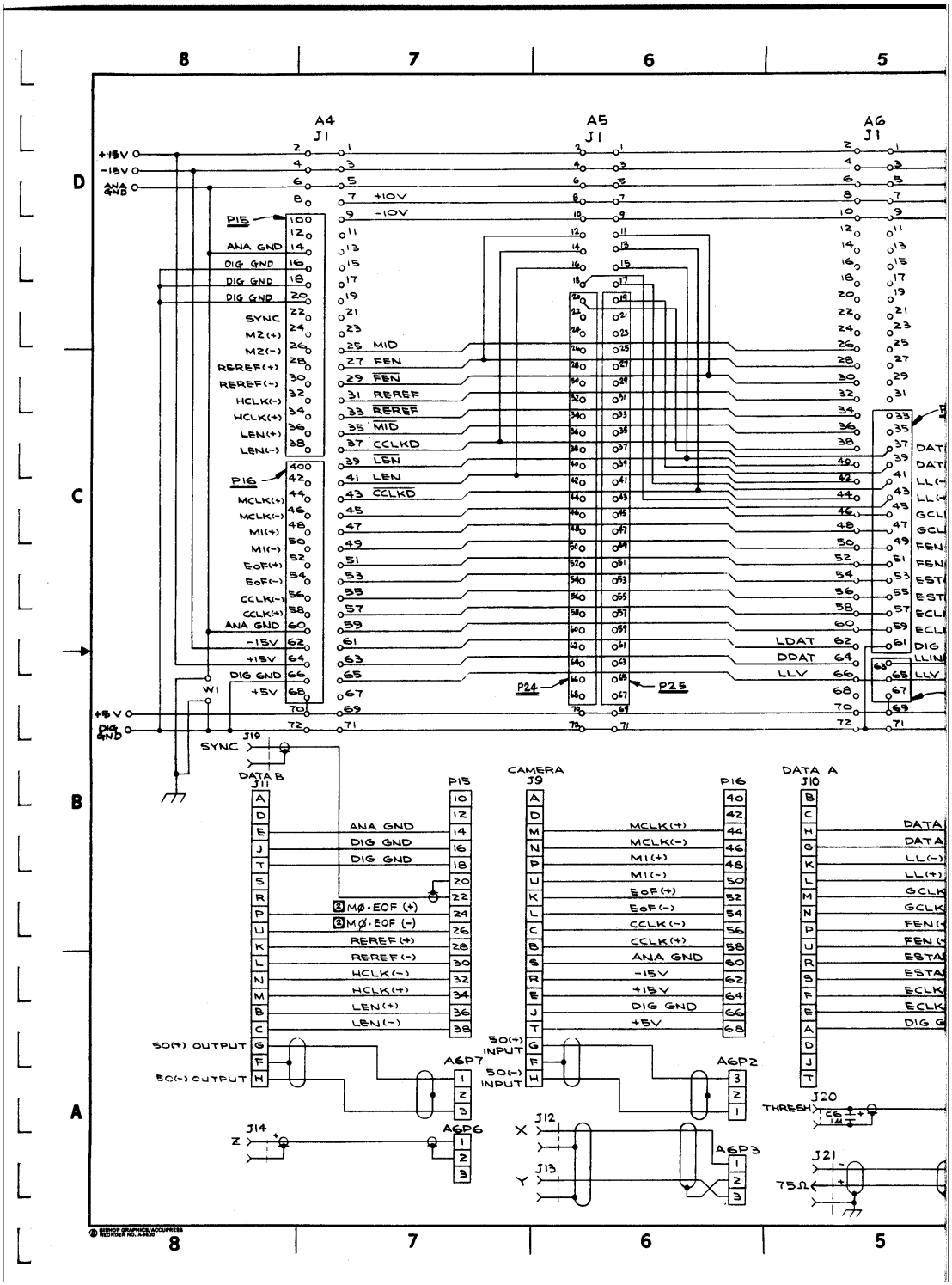
SCALE TWICE | SHEET 1 OF 1

NEXT ASSY	USED ON
APPLICATION	

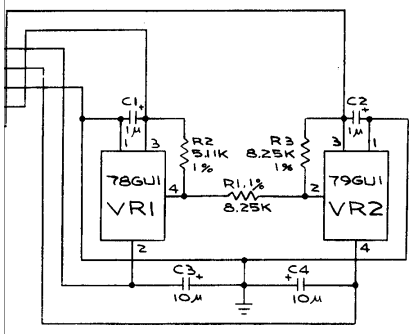
12-14


LEN
LEN
WID
CCLKD
ODD P.W. ADJ
EVEN P.W. ADJ
75361A
90Ω VIDEO INPUT
C-BAL ADJ
R-BAL ADJUST
RECEIVE GAIN ADJUST
C FINE BAL ADJ
LM1496N
MPS6515
MPS6519
MMH0026
SD210
RRHV
LENHV
RRB
FEN
AMPLITUDE ADJ
REF DESIGS
HIGHEST USED
NOT USED
R184
C141
U33
Q22
TP11
WT
P5
CR1
NOTES: (UNLESS OT
1. RESISTORS AR
CAPACITORS A
DEPENDING ON


REVISIONS
ZONE | LTR | DESCRIPTION | DATE | APPROVED
A | REVISED | 9-3-76 | JV
U11 LM1496N
U29 LM1496N
U27 LM361N
U28 LM361N
U9 356N
U10 356N
U33 356
U12 LH0002CH
U13 LH0002CH
U14 LH0002CH
U15 LH0002CH
U23 LH0002CH
U24 LH0002CH
U25A 7474
U25B 7474
U26A 7474
U26B 7474
U31 LM741CN
U30A 9638TC
U30B 9638TC
U32A 7404
U32B 7404
U32C 7404
U32D 7404
Q11 MPS6515
Q12 MPS6515
Q13 MPS6515
Q22 MD8001
Q20 SD210
Q21 SD210
Q14 SD210
SD210
1N914
+10V
-10V
+15V
-15V
+5V
LEN
BLANK BALANCE
DARK LEVEL ADJ
TRANSMIT BALANCE ADJUST
TRANSMIT GAIN ADJUST
DATA THRESHOLD ADJUST
WEN LEN CCLKS
P1 37 DATA(+)
39 DATA(-)
62 LDAT
41 LL(-)
43 LL(+)
P3 1 X
2
3 Y
P1-65,66 LLV
P1-64 DDAT
P4
P5
P6
P7
P8
(SPECIFIED)
5, 1/4 W, 5%.
ICROFARADS.
115 & 116 ARE OPTIONAL
CABLE LENGTH.
QTY REQD | CODE IDENT | PART OR IDENTIFYING NO. | NOMENCLATURE OR DESCRIPTION
PARTS LIST
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES TOLERANCES ARE FRACTIONS DECIMALS ANGLES
MATERIAL
FINISH
NEXT ASSY | USED ON
APPLICATION
DO NOT SCALE DRAWING
CONTRACT NO.
APPROVALS | DATE
DRAWN DOUGLAS V PAH | 4-14-76
CHECKED | 5-3-76
5-10-76
5-10-76
RETICON CORPORATION
SCHEMATIC
ANALOG BOARD
RS 520
SIZE E | CODE IDENT NO. | DRAWING NO. 011-0225 | REV A
SCALE | SHEET 1 OF 1

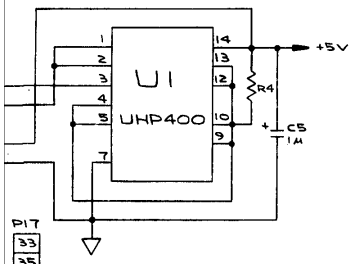

A4 J1
A5 J1
A6 J1
+15V
-15V
ANA GND
DIG GND
+5V
+10V
-10V
P15
P16
SYNC
MID
FEN
REREF
CCLKD
LEN
MCLK(+)
MCLK(-)
M1(+)
M1(-)
EOF(+)
EOF(-)
CCLK(-)
CCLK(+)
HCLK(-)
HCLK(+)
LEN(+)
LEN(-)
REREF(+)
REREF(-)
M2(+)
M2(-)
LDAT
DDAT
LLV
P24
P25
W1
J19
J11
DATA B
J15
CAMERA
J9
P16
DATA A
J10
MØ·EOF (+)
MØ·EOF (-)
50(+) OUTPUT
50(-) OUTPUT
50(+) INPUT
50(-) INPUT
A6P7
A6P2
A6P6
A6P3
J14
J12
J13
J20
J21
THRESH
75Ω
X
Y
Z

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVED
	A	REVISED	4-24-78	
	B	INCORP ECO #596	4-26-79	6-26-79
	C	INCORP ECO #655	12-18-79	



NOTES:

1. INSERT P2 THRU P8 WITH PLUG NO. TOWARD TOP OF CONTROLLER.
2. ON CONTROLLERS WITH S/N 78083 THRU 78091 INDICATED OUTPUT WAS M2(+) & M2(-) SIGNAL.



P25		A/D J'23
29	- DATA RDY	29
31	- STATUS	31
33	- CONVERT	33
35	- 128 ODD	2
37	- 64 ODD	4
39	- 32 ODD	6
41	- 16 ODD	8
43	- 8 ODD	10
45	- 4 ODD	12
47	- 2 ODD	14
49	- 1 ODD	16
51	- 128 EVEN	35
53	- 64 EVEN	37
55	- 32 EVEN	39
57	- 16 EVEN	41
59	- 8 EVEN	43
61	- 4 EVEN	45
63	- 2 EVEN	47
65	- 1 EVEN	49
67	DIGITAL GND	50

P24		
30	+ DATA RDY	28
32	+ STATUS	30
34	+ CONVERT	32
36	+ 128 ODD	1
38	+ 64 ODD	3
40	+ 32 ODD	5
42	+ 16 ODD	7
44	+ 8 ODD	9
46	+ 4 ODD	11
48	+ 2 ODD	13
50	+ 1 ODD	15
52	+ 128 EVEN	34
54	+ 64 EVEN	36
56	+ 32 EVEN	38
58	+ 16 EVEN	40
60	+ 8 EVEN	42
62	+ 4 EVEN	44
64	+ 2 EVEN	46
66	+ 1 EVEN	48
68	DIGITAL GND	17

P17: 33, 35, 37, 39, 41, 43, 45, 47, 49, 51, 53, 55, 57, 59, 61

AGP18: 63, 65, 67 — DS1 LIGHT LEVEL

AGP4: 3, 2, 1

AGP8: 1, 2, 3

12-16

QTY REQD	CODE IDENT	PART OR IDENTIFYING NO.	NOMENCLATURE OR DESCRIPTION
			PARTS LIST

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS ± DECIMALS .XX ± .XXX ± ANGLES ±

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN DBJNIS YGH	1-9-78
CHECKED	5-3-78
	5.10.78
T.Sherman	5-11-78

RETICON
AN EMRAD COMPANY
RETICON CORPORATION
910 Benicia Ave.
Sunnyvale
California 94086

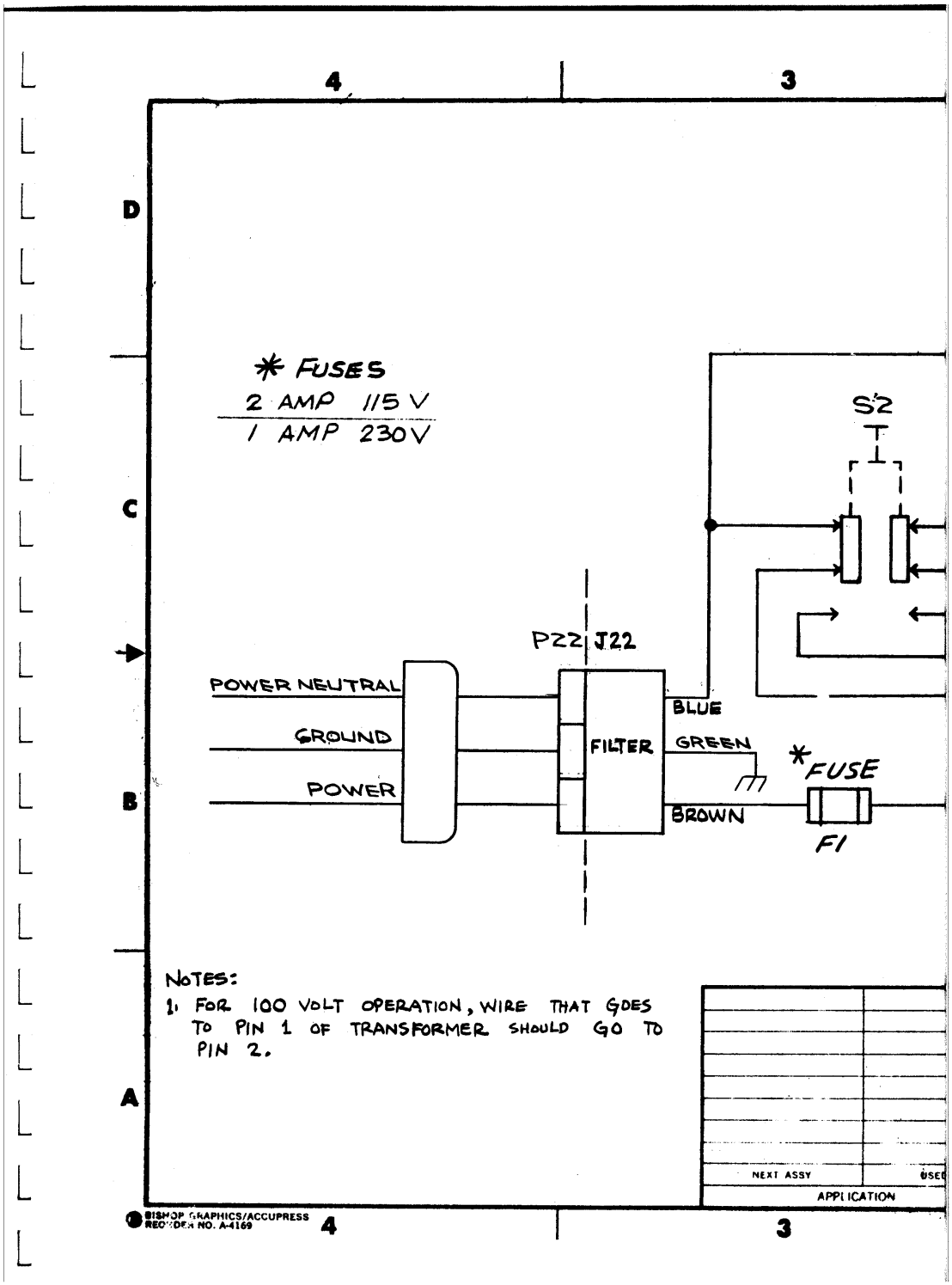
INTERCONNECT DIAGRAM
RS 520 CONTROLLER

SIZE	CODE IDENT NO.	DRAWING NO.	REV
D		022-0063	C

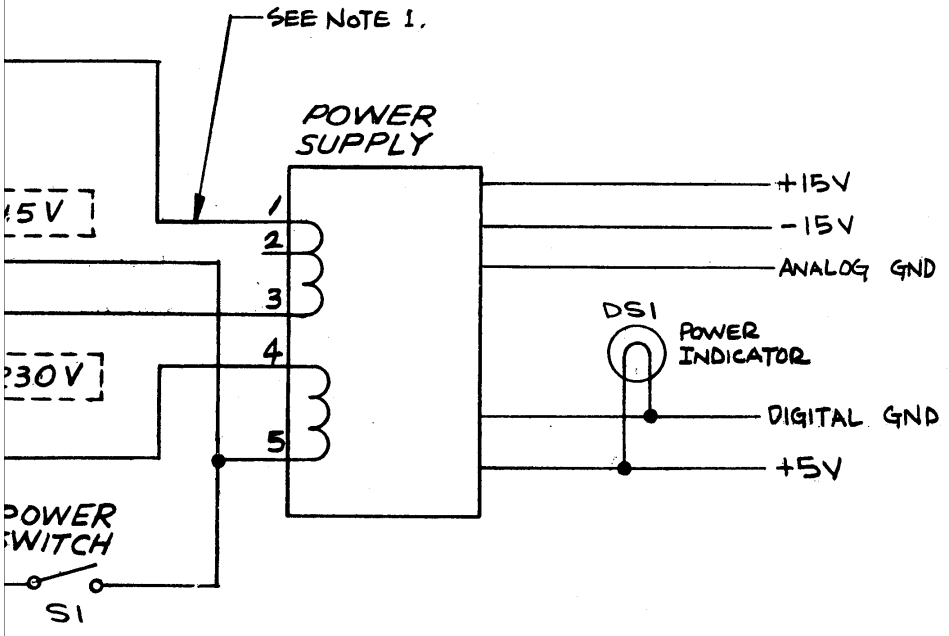
SCALE

SHEET 1 OF 1

NEXT ASSY	USED ON
APPLICATION	


4
3
D
C
B
A
* FUSES
2 AMP 115 V
1 AMP 230V
S2
P22 J22
POWER NEUTRAL
GROUND
POWER
FILTER
BLUE
GREEN
BROWN
*FUSE
F1
NOTES:
1. FOR 100 VOLT OPERATION, WIRE THAT GOES TO PIN 1 OF TRANSFORMER SHOULD GO TO PIN 2.
NEXT ASSY
USED
APPLICATION
BISHOP GRAPHICS/ACCUPRESS
REORDER NO. A-4169
4
3

REVISIONS				
ZONE	LTR	DESCRIPTION	DATE	APPROVAL
	A	INCORP ECO#607	7-24-79	TB



UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES
TOLERANCES ARE:
FRACTIONS DECIMALS ANGLES
± .XX ± °
.XXX °

MATERIAL

FINISH

DO NOT SCALE DRAWING

CONTRACT NO.

APPROVALS	DATE
DRAWN T. Shannon	3.14.78
CHECKED Eg Wa	4-25-78
	4-25-78
	4.25.78
T. Shannon	4.25.78

RETICON

RETICON CORPORATION
910 Benecia Ave.
Sunnyvale
California 94086

POWER DISTRIBUTION DIAGRAM, RS520

SIZE	CODE IDENT NO.	DRAWING NO.	
B		023-0116	A

SCALE | SHEET | OF |

12-17

SECTION XIII

LIST OF PHOTOGRAPHS

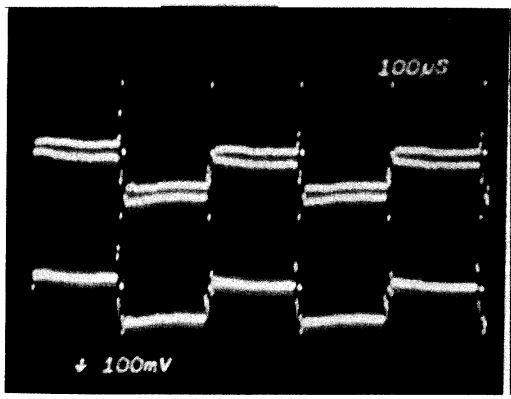


Photo 1

Upper trace - Pixel and Line Offset

Lower trace - Line Offset

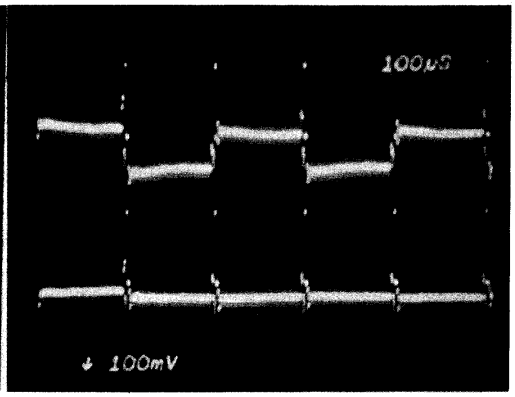


Photo 2

Upper trace - Line Offset

Lower trace - Line Offset Balanced

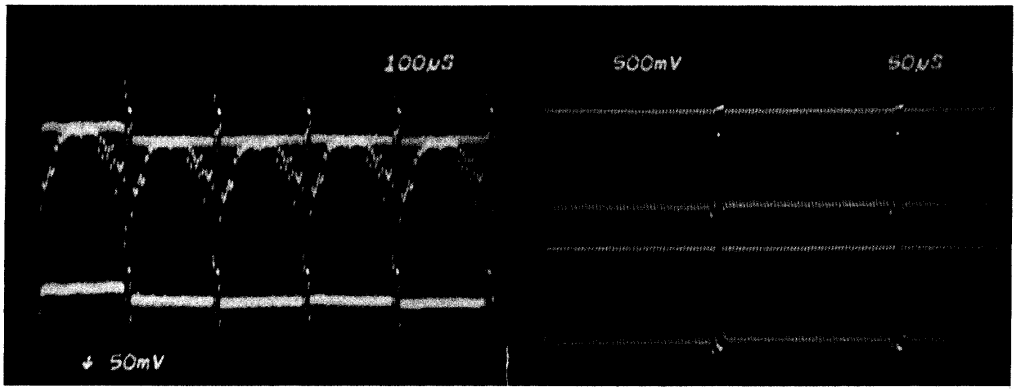


Photo 3

Upper trace - LR/LT Offset

Lower trace - LR/LT Balanced

Photo 4

Upper trace - Even Array Video

Lower trace - Odd Array Video

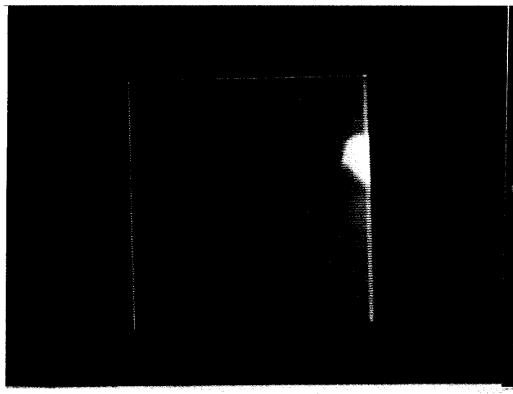


Photo 5

Light Spot Raster

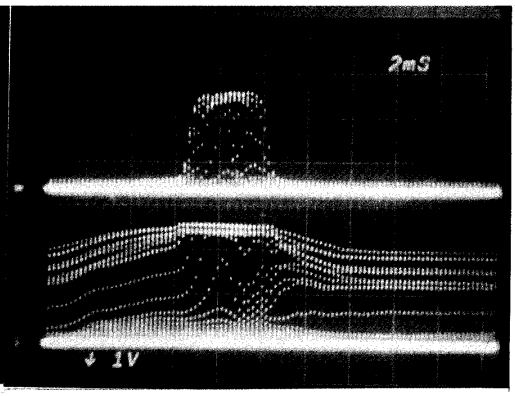


Photo 6

Upper trace - Light Spot Video

Lower trace - 100% Blooming

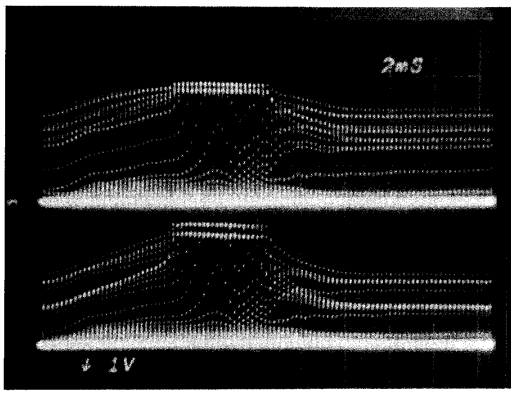


Photo 7

Upper trace - 100% Blooming

Lower trace - Blooming Minimized

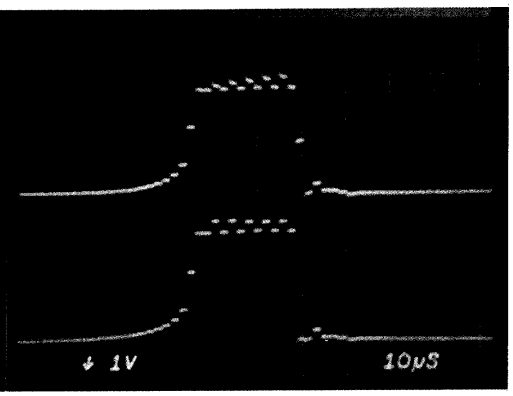


Photo 8

Upper trace - D1 Pixel Offset

Lower trace - D1 Offset Minimized

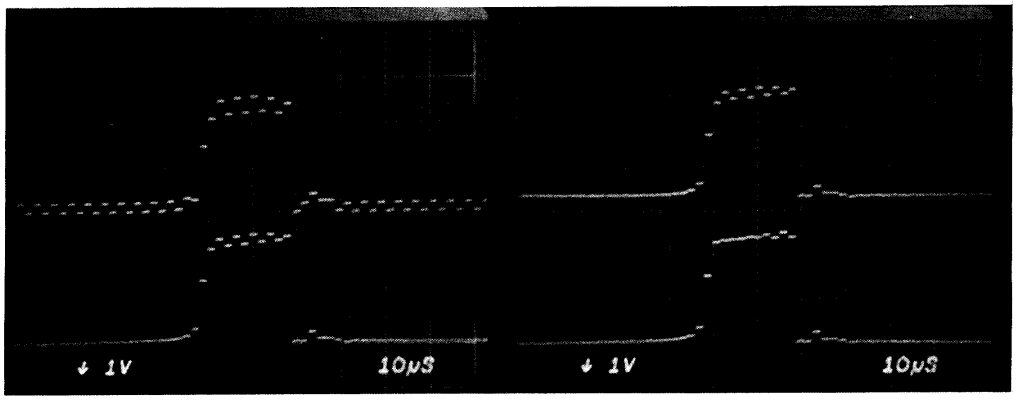


Photo 9

Upper trace - Dark and Light Offset

Lower trace - Light Offset

Photo 10

Upper trace - Light Offset

Lower trace - Dark and Light Offset Minimized

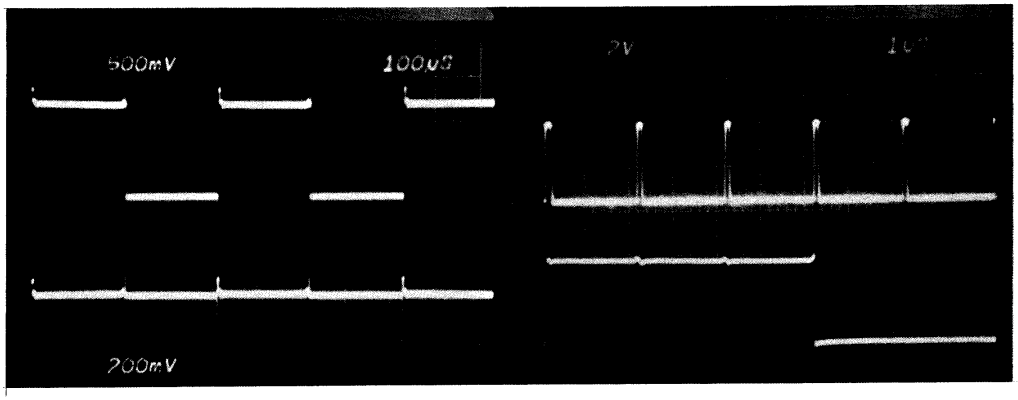


Photo 11

Upper trace - Viris Unbalanced

Lower trace - Viris Balanced

Photo 12

Upper trace - Mclk Pulses

Lower trace - M1 Pulse

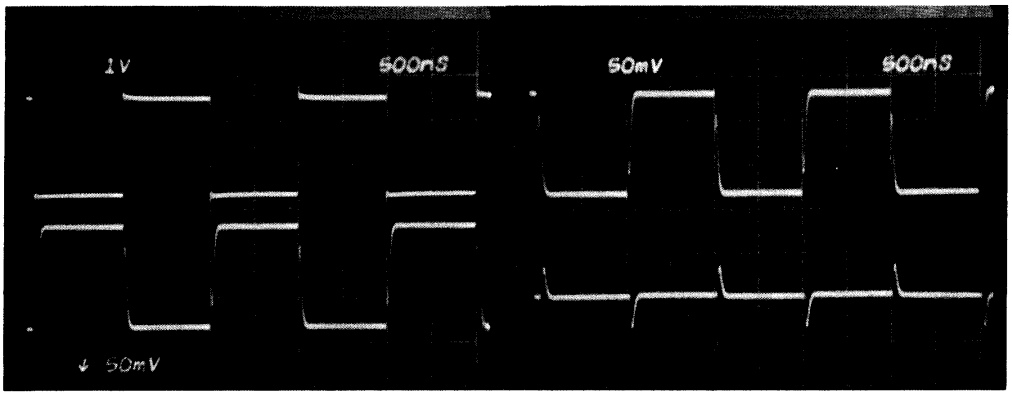


Photo 13

Upper trace - 500KHz Square Wave

Lower trace - Receiver R Unbalanced

Photo 14

Upper trace - Receiver R Unbalanced

Lower trace - Receiver R Balanced

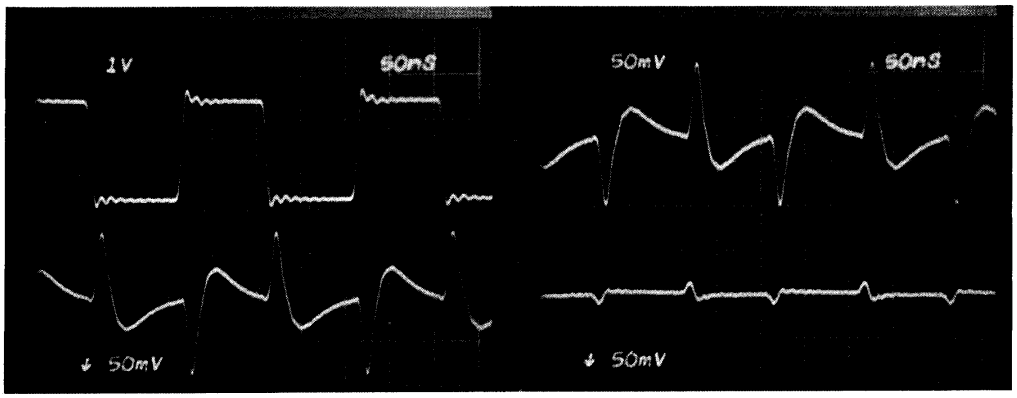


Photo 15

Upper trace - 5MHz Square Wave

Lower trace - Receiver C Unbalanced

Photo 16

Upper trace - Receiver C Unbalanced

Lower trace - Receiver C Balanced

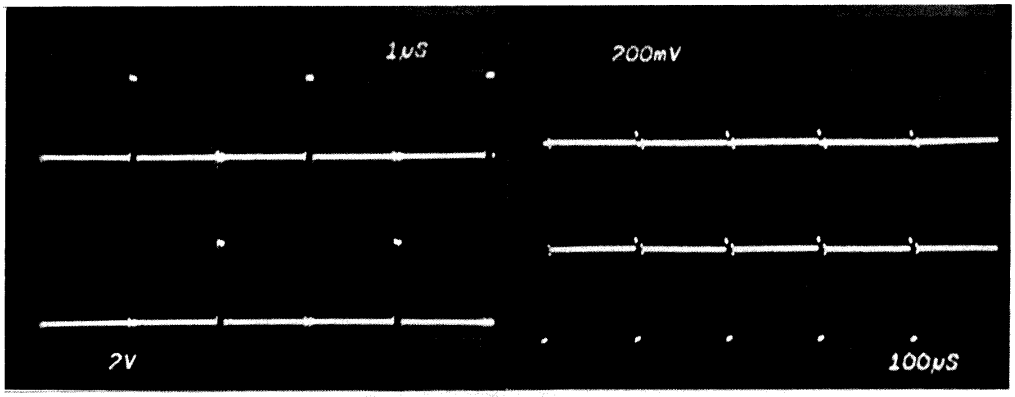


Photo 17

Upper trace - Odd Sample Pulse

Lower trace - Even Sample Pulse

Photo 18

Upper trace - Dark and Blanking Level Zero Volt

Lower trace - Dark Level Zero Volts,
Blanking Level - 400 Millivolts

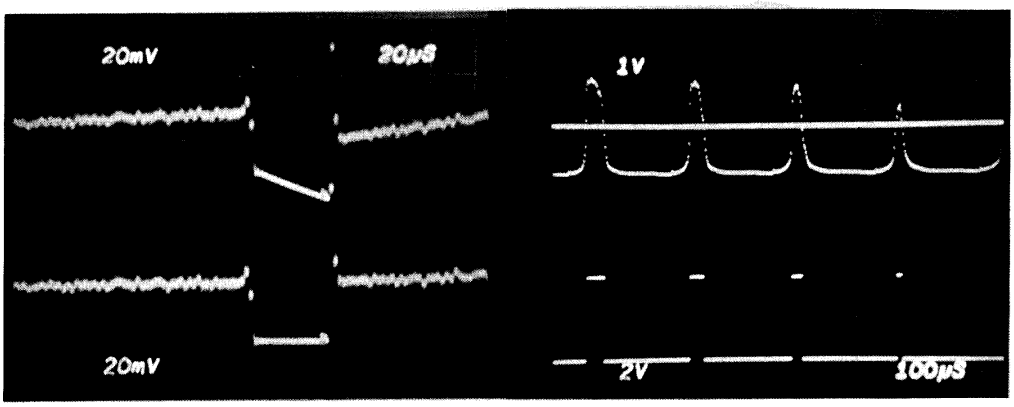


Photo 19

Upper trace - Blanking Unbalanced

Lower trace - Blanking Balanced

Photo 20

Upper trace - Video and Threshold Levels

Lower trace - Binary Data Response