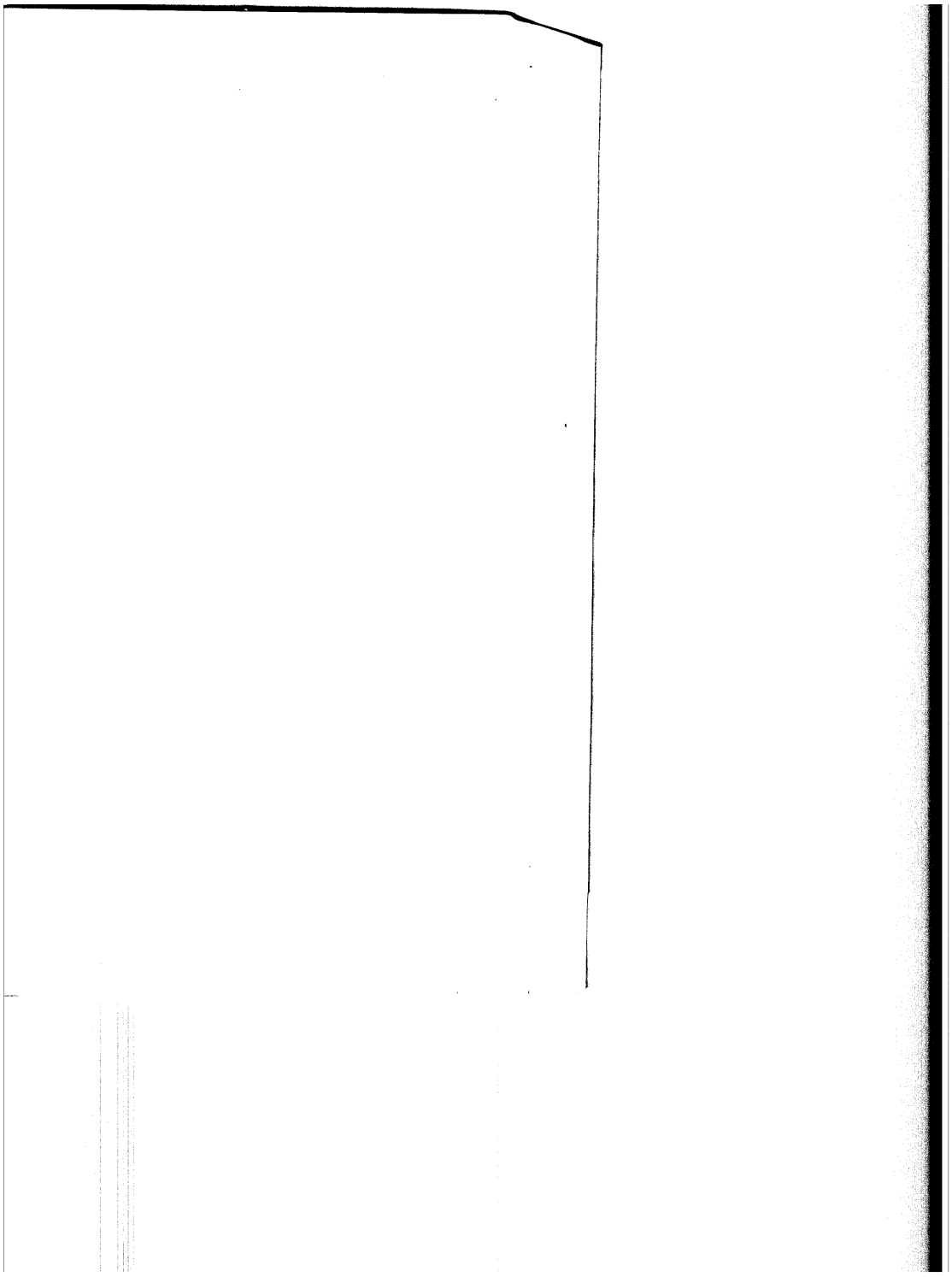
The S-100
and
Other Micro Buses



Preface

Everyone's computer seems to shrink with age. This shrinkage is usually first apparent in the memory as what was, initially, an enormous memory becomes very confining. The addition of another memory board or two temporarily solves the problem. Also, at first, the lack of hardcopy seems almost a blessing but, with every passing clock cycle, the need for a written record becomes more important. A printer interface board is added in hopes that it will do the trick. However, there are a host of expansion boards available for expansion and the present system always seems to be wanting and waiting for more and more. The key to system expansion is the *bus* through which the processor communicates with the present and future system components.

This book is about buses. A general discussion in Chapter 1 is used to acquaint the reader with bus basics. Then, the mechanical data, pinout designations, and bus signal definitions of the 11 most widely used bus systems are listed and explained in the following chapters so that the reader may better understand the bus of his or her system, or evaluate the bus of another system, or plan the interface of one bus to another. Expansion and interface boards are described and explained so that a greater use of the bus system can be obtained. Many photographs and pinout drawings are shown so that a better understanding of microcomputers, interface boards, and *buses* can be realized.

We would like to express our appreciation to the many manufacturers who participated in the preparation of this book by sharing their schematics and system descriptions. Thus, they have helped the reader to better understand and use their products. We also want to give special thanks to Debbie for her meritorious service in preparing the manuscript.

Contents

CHAPTER 1

Bus Structures

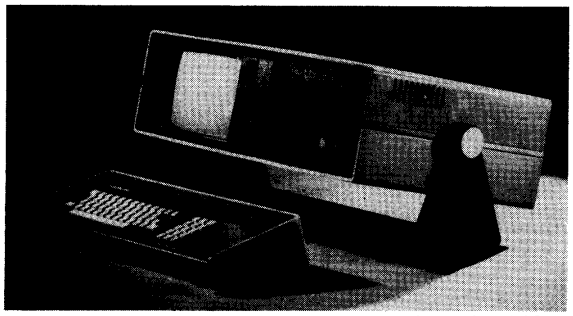
After the introduction of the Altair 8800 in early 1975, interest in microcomputers by hobbyists began to grow rapidly. In those early days, getting a system set up and running was often a formidable challenge. Yet, even then, the need for system expansion was quickly felt. Companies producing Altair-compatible memory boards soon appeared and flourished. By the end of the year, the Altair had become a leader with over 50 companies producing plug-compatible boards for the "Altair" or S-100 bus. During this period, several other successful systems, including the SWTP 6800, KIM-1 and IMSAI, were introduced. Some of these systems used the Altair bus but many did not. Since then, many systems and buses have appeared. Memory, serial and parallel I/O, video and graphics display, analog I/O, voice systems and recognition, music synthesis, and a host of other boards are available for these systems. Figs. 1-1 through 1-9 show some typical systems and plug-in boards.

The Commodore PET shown in Fig. 1-1 is a complete microcomputer system in one unit. It has its own bus. The Bytemaster illustrated in Fig. 1-2 is also a complete microcomputer system with its own bus. The SOL-20 computer shown in Fig. 1-3 has an S-100 bus system containing several slots for expansion but it lacks a video monitor. The Heathkit H8 uses Heath's Benton Harbor Bus. It is complete as shown in Fig. 1-4 using keypad and octal displays or it is usable with other I/O devices.

Fig. 1-5 shows the Vector 1, an S-100-based system that relies entirely on external I/O devices. An S-100 Serial Communications Board is illustrated in Fig. 1-6, while a Heath H8-2 Parallel Interface Board is shown in Fig. 1-7. Notice the bus connector on the right side of the H8-2 board. Fig. 1-8 shows the Percom Floppy

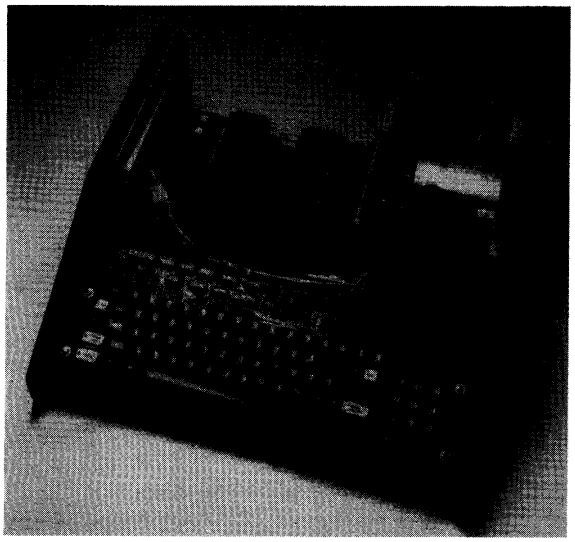
Courtesy Commodore Business Machines, Inc.

Fig. 1-1. PET, a complete microcomputer system.



Courtesy The Digital Group

Fig. 1-2. BYTEMASTER, a complete microcomputer system.



Courtesy Processor Technology Corp.

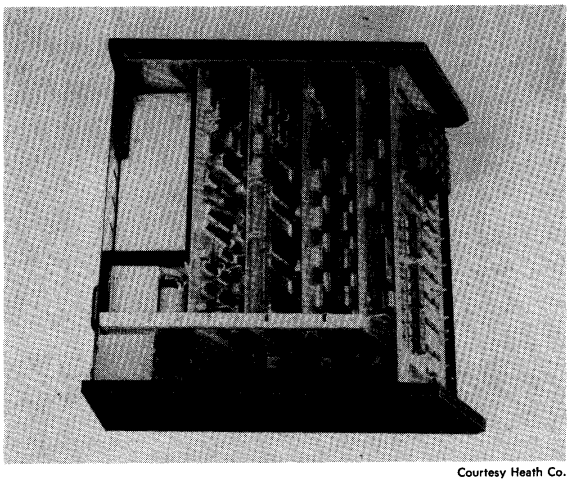
Fig. 1-3. Sol-20 computer (inside view).

Disk and Controller for SS-50 systems, while Fig. 1-9 illustrates the Video Digitizer Board. It is using the SS-30 connector in an SS-50 system.

The bus of a system is the selection and arrangement of its signal and power lines on a connector for distribution to other boards. Bus structure becomes important when system expansion is considered, since the needed signals must be available. Careful examination of the bus of a system should be made before a system is purchased. The most popular buses will be subsequently discussed in detail.

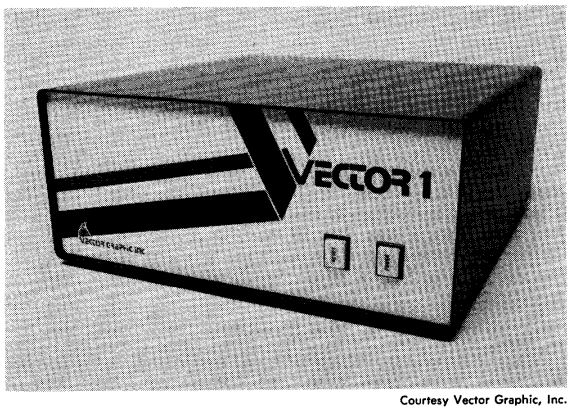
ADDRESS LINES

Regardless of the microprocessor used in a system or the number of lines on its bus, the address, data, and control signals must be available. The address lines are used by the processor to indicate to memory and other peripherals the location with which it wants



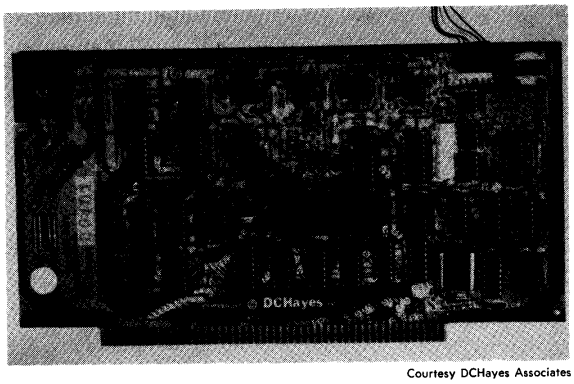
Courtesy Heath Co.

Fig. 1-4. Heathkit H8 digital computer mainframe.



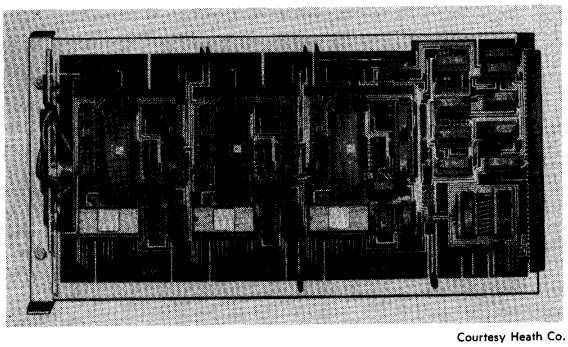
Courtesy Vector Graphic, Inc.

Fig. 1-5. VECTOR 1 is an S-100-based system.



Courtesy DCHayes Associates

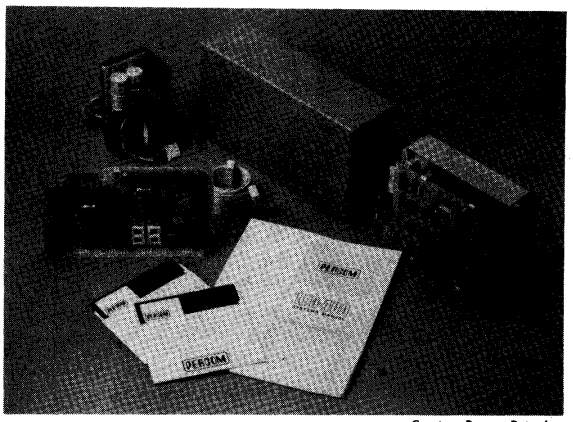
Fig. 1-6. An S-100 serial communications board.



Courtesy Heath Co.

Fig. 1-7. Heath H8-2 parallel interface board.

to communicate. The 8080, Z80, 6800 and 6502 have 16 address lines, generally labeled A0–A15, that are divided into two 8-bit bytes. Lines A0–A7 comprise the low-address byte and lines A8–A15 comprise the high-address byte. Not all address lines may be used by any one board.



Courtesy Percom Data, Inc.

Fig. 1-8. Percom floppy disk and controller for SS-50 systems.

DATA LINES

The eight data lines, usually designated D0–D7, carry instructions and data between the processor and all the peripherals, including the memory. All processors have bidirectional data lines which carry information both into and out of the processor. The direction of information flow on these lines is usually under processor control. All buses, except the S-100 and the Digital Group, maintain the bidirectional data lines. The S-100 splits the data lines into eight data-input and eight data-output lines. The Digital Group splits them into eight memory-data in, eight memory-data out, eight I/O in and eight I/O out.

CONTROL LINES

The control lines coordinate the operations of all system components. Most buses include a master clock line, often $\phi 2$ on the processor, that indicates to peripherals that the address placed on the bus is settled and valid. The master clock line also indicates valid data is on the data lines during a Write operation and that the processor can accept data placed on the data lines during a Read operation. The 8080 and Z80 buses may include an M1 line that

Courtesy The Micro Works

Fig. 1-9. Video digitizer board using the SS-30 connector in an SS-50 system.

signals the beginning of an op code fetch and a sync line that signals the beginning of each machine cycle.

Direction of data flow on the data lines is determined by one or more processor outputs. The 6800 and 6502 systems use a single Read/Write line to control data direction. When the line is high, a Read operation is indicated, when low, a Write operation will occur. The 8080- and Z80-based systems use separate Read and Write lines and they separate memory from other I/O with two sets of control lines. The Memory-Read and Memory-Write lines control direction of data flow during memory operations. The I/O Read and Write lines control data direction during I/O operations. Most buses include a ready line that can be used by slow memory or I/O to momentarily halt the processor until valid data can be accessed.

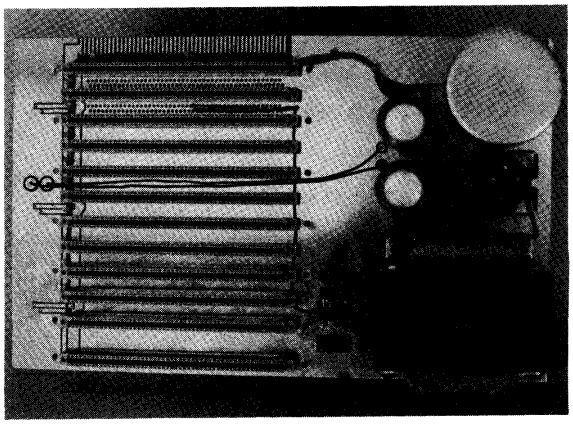
Most buses include Reset lines. Although a few of these are connected directly to the processor's Reset input, many are not. Some are outputs of a reset pulse generator that can be used to reset peripherals. Others are inputs to circuitry that reset the operating system, often through a nonmaskable Interrupt input, without resetting the processor.

Interrupt inputs are common to all systems. These inputs allow in-

frequent or important peripherals to get the attention of the system. A maskable Interrupt input line can be ignored by the processor on direction from the program. A nonmaskable input cannot be ignored, it must be serviced by the processor. Vectored Interrupt inputs feed an interrupt controller that assigns priority if more than one interrupt request should occur at one time. The number and type of Interrupt inputs varies widely among buses. The 8080 and Z80 buses may include status lines that indicate the condition of the maskable input or acknowledge the processor's recognition of an interrupt request.

The DMA operations are facilitated on most buses by the inclusion of bus disable lines. These lines are inputs that will cause some or all of the bus lines of the processor to enter a high-impedance state, which effectively disconnects them from the bus. An external device can then control the buses for Memory-Read and -Write operations. A status line signals that the buses have been floated and the DMA can begin.

All processors require at least +5 volts dc. The 8080 also needs −5 and +12 volts dc. PROMs and communications devices may need −5, −9, or −12 volts. Most buses supply these voltages as filtered but unregulated +8 and ±16 volts, with regulation occurring on the individual boards.



Courtesy Quay Corp.

Fig. 1-10. A 12-slot expandable S-100 motherboard.

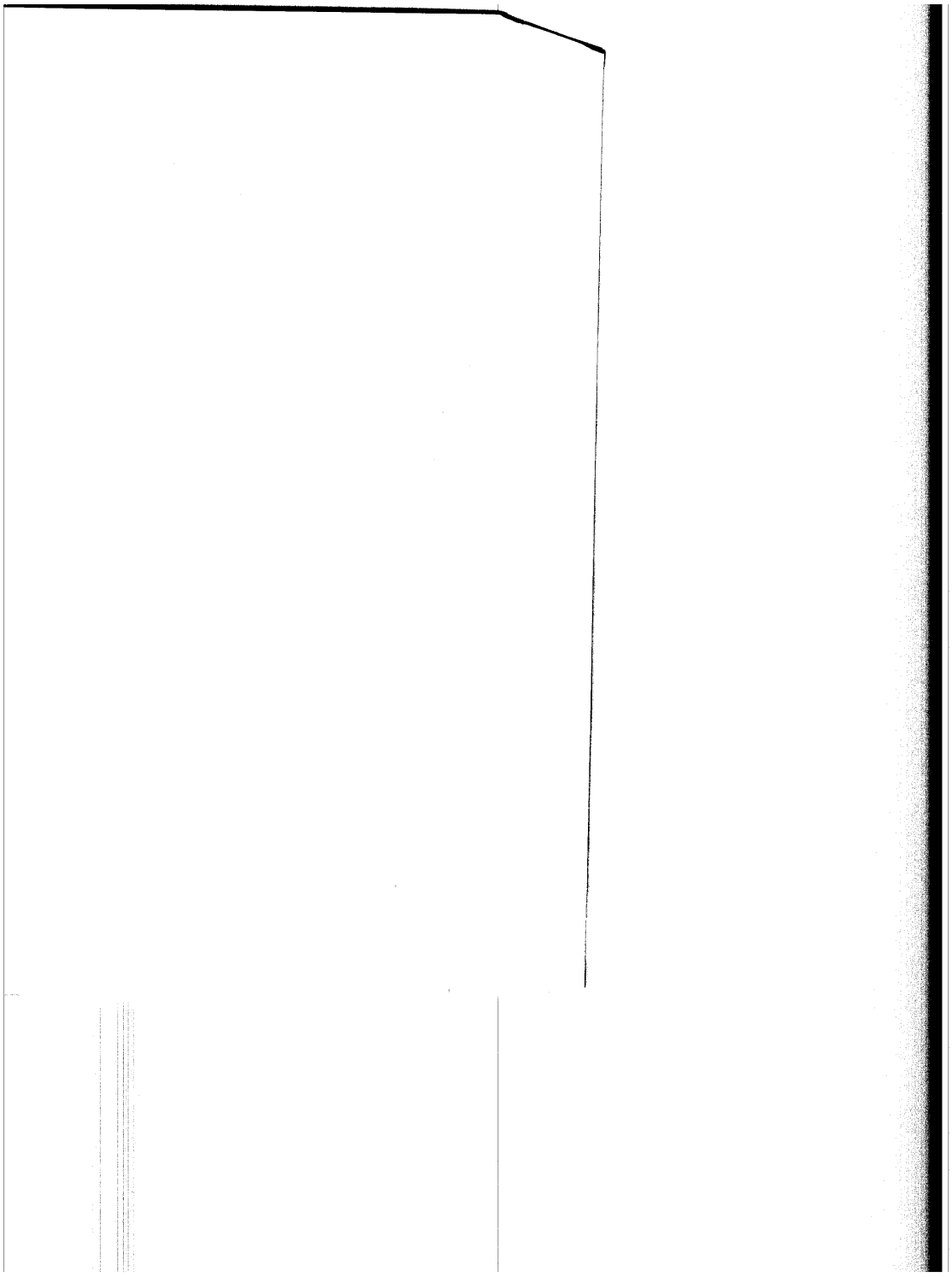
SYSTEM EXPANSION

Expansion of systems occurs via a motherboard as shown in Fig. 1-10. A motherboard is a printed-circuit board that distributes bus signals to several connectors which mate with system boards. Motherboards are an integral part of some systems but single-board computers may require their addition to allow for expansion. Adding a board to a system is not as simple as just purchasing it and plugging it in. A space must be available on the motherboard; indeed, a motherboard must be present. The power supply of the system must produce the necessary voltages and be able to provide the extra current required by the new board. The power requirement may become critical in a system that is presently expanded.

The microprocessor board of the system must be able to electrically drive the devices on the new board. The processor has very limited drive capabilities so most systems pass the signals of the processor through buffer chips. These devices provide little load on the processor and are capable of driving up to 100 other devices. Without buffering, the processor can be fatally damaged. However, if a system does not buffer the signals of the processor, a buffer board may have to be added. Also, the speed of the new board must be compatible with the system. Memory and peripherals may not be able to respond to the timing demands of the processor. Although most systems include the Ready input to temporarily slow the processor, this may be unacceptable.

Care should be taken when assigning addresses to the newly added boards. New boards must be placed in unused locations. The memory map of the system can be examined to determine the locations of existing boards and possible addresses for the new boards.

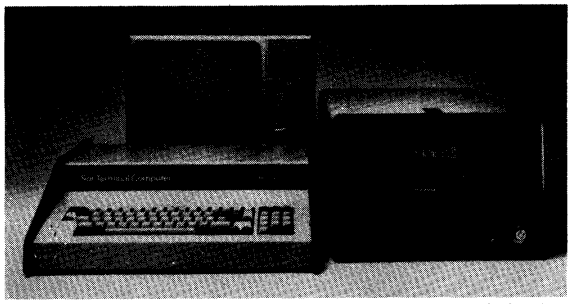
Finally, plug compatibility must be carefully examined. A board designed for one bus will not plug directly into another but bus interface boards are commercially available. Yet, compatibility problems exist between boards that are built for the same bus. The old rule of buying the processor and all additional boards from the same company no longer holds true. The pinout and signal definitions for both the system and the new board should be examined before the purchase is made. Specifications of the most popular buses are listed and explained in the following pages.



CHAPTER 2

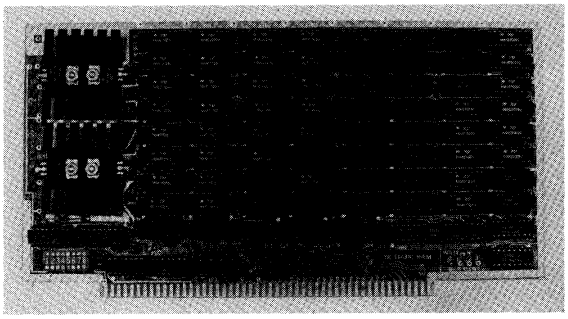
The S-100 Bus

The S-100 bus was introduced by MITS Inc. on their 8080-based Altair kit. In fact, many of the bus lines are signals which are generated by the 8080 processor. It has become the most popular bus, if not the industry standard, in use by hobbyists today. Fig. 2-1 shows an S-100 microcomputer system which includes a keyboard, video monitor, and dual floppy disk. There are more than 300 boards being advertised as directly compatible with the S-100 bus. These include a multitude of memory boards, serial and parallel interface boards, floppy disk controller boards, video boards, music



Courtesy Processor Technology Corp.

Fig. 2-1. Sol System III microcomputer system.

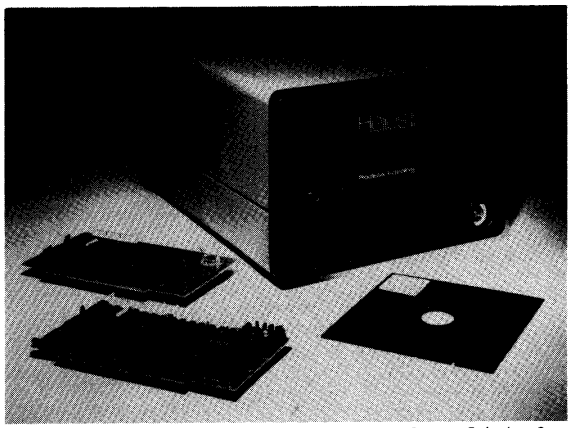


Courtesy Quay Corp.

Fig. 2-2. A memory board (8K static RAM).

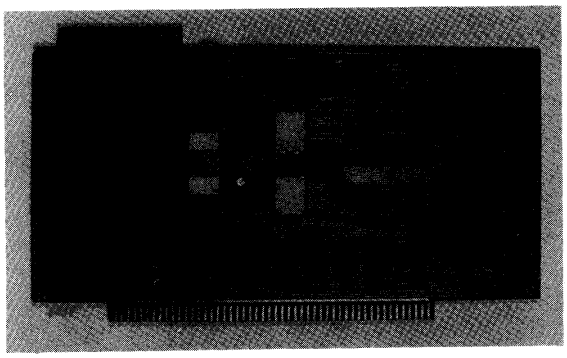
synthesizer boards, and speech recognition boards. Some examples are shown in Figs. 2-2 through 2-5.

The standard S-100 circuit board (e.g., Fig. 2-2) has overall dimensions of 5.3 inches by 10 inches. It fits into a 100-pin edge con-



Courtesy Processor Technology Corp.

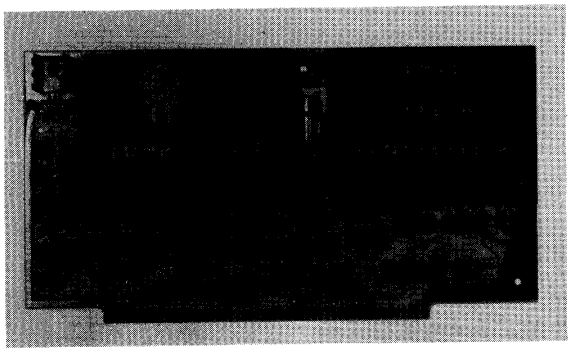
Fig. 2-3. A floppy disk with control boards.



Courtesy Xitex Corp.

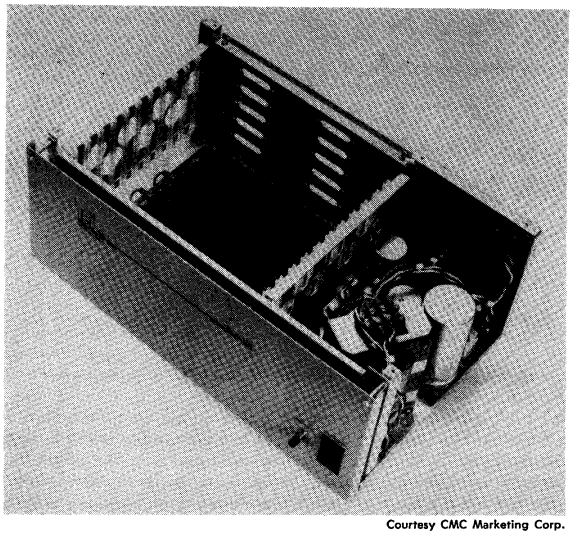
Fig. 2.4. Stand-alone video board. Only +7 V dc and GND on the bus are used.

nector (50 on each side spaced 0.125 inch apart) on a motherboard (Fig. 2-6). The pins are numbered from left to right as seen in Fig. 2-2 with pins 1–50 on the component side and pins 51–100 on the opposite side. The bus supplies unregulated voltages to the boards; therefore, all boards must contain the necessary regulators. The pins are offset toward one end so that the boards cannot be inserted backwards. The S-100 pinout designations are listed in Fig. 2-7.



Courtesy Computalker Consultants

Fig. 2-5. Speech synthesizer board.



Courtesy CMC Marketing Corp.

Fig. 2-6. S-100 mainframe including chassis, 12-slot motherboard and power supply.

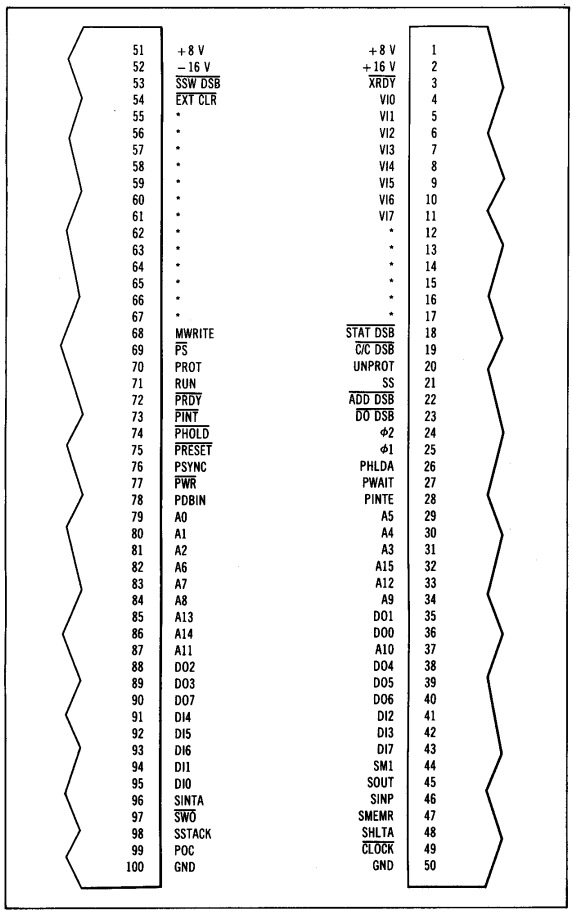


Fig. 2-7. S-100 pinout designations.

S-100 SIGNAL DEFINITIONS

Pin No.	Signal	Definition
1	+8 V	Unregulated input to +5 V regulators
2	+16 V	Positive unregulated voltage supply
3	$\overline{\text{XRDY}}$ (READY 1)	External Ready—ANDed with $\overline{\text{PRDY}}$ (pin 72) and connected to READY on the 8080. If $\overline{\text{XRDY}}$ and/or $\overline{\text{PRDY}}$ are pulled low, the CPU will enter a Wait state until both are high. XRDY is often used as a front panel control and can allow single stepping. $\overline{\text{PRDY}}$ usually is used to signal when valid data from slow memory is on the bus.
4	VI0	Vectored Interrupt 0—A vectored interrupt system is used when very fast multiple interrupt response is required and is implemented with a special circuit card.
5	VI1	Vectored Interrupt 1
6	VI2	Vectored Interrupt 2
7	VI3	Vectored Interrupt 3
8	VI4	Vectored Interrupt 4
9	VI5	Vectored Interrupt 5
10	VI6	Vectored Interrupt 6
11	VI7	Vectored Interrupt 7
12*	XRDY 2	External Ready 2
	$\overline{\text{NMI}}$	Nonmaskable Interrupt
	+12 V	Battery backup
	READY 3	
13*	$\overline{\text{IRQ}}$	Interrupt Request
	CK3	Phase 3 shift clock
	STDBY	Standby power
	PAUSE	—
	—	Bank Select 8
14*	RDS BL/L	Phase
	ϕ1	M6800 Phase 1 clock
	CK1	Phase 1 shift clock
	STDBY	Standby power
	—	Bank Select 9
	OPREQ	
15*	ϕ2	M6800 Phase 2 clock
	$\overline{\text{BWE}}$	Write Enable ANDed with Write
	NMI	Nonmaskable Interrupt
	—	Battery backup
	—	Bank Select 10/Address 18
	$\overline{\text{STOP CLK}}$	
16*	R/W	M6800 Read/Write
	LDM	Load Medium Address Byte
	—	Bank Select 11/Address 16
	INTAK	
17*	BDSEL	Acknowledge signal from addressed memory board
	$\overline{\text{NMI}}$	Nonmaskable Interrupt

Pin No.	Signal	Definition
	BGNT+	CPU Bus Grant
	—	Bank Select 12/Address 17
18	$\overline{\text{STAT DSB}}$	Status Disable—A low on this line puts the 8 status line buffers (SMEMR, SINP, SMI, SOUT, SHLTA, SSTACK, SWO, and SINTA) into a high impedance state.
19	$\overline{\text{C/C DSB}}$	Command/Control Disable—A low on this line puts the 6 command/control line buffers (PHLDA, PSYNC, PDBIN, PINTE, $\overline{\text{PWR}}$, and PWAIT) into a high impedance state.
20	UNPROT	Unprotect—A positive pulse resets the Protect flip-flop on the currently addressed board so that it can accept data. A positive pulse on PROT (pin 70) sets the flip-flop so that data cannot be written into the currently addressed memory board. Protect Status ($\overline{\text{PS}}$, pin 69) indicates the flip-flop status; low for Protect and high for Unprotect.
21	SS	Single Step—Used by front panel, a high disables input buffer while panel drives bidirectional data bus.
22	$\overline{\text{ADD DSB}}$	Address Disable—A low on this line puts the 16 address line buffers into a high impedance state.
23	$\overline{\text{DO DSB}}$	Data Out Disable—A low on this line puts the 8 data line buffers into a high impedance state.
24	$\phi 2$	Phase 2 clock—The master timing signal for the bus.
25	$\phi 1$	Phase 1 clock
26	PHLDA	Halt Acknowledge—Processor command/control output signal which goes high in response to the HOLD signal. It indicates that the data and address buses will go to the high impedance state and the processor (8080) will enter HOLD state after completion of current machine cycle. Note: $\overline{\text{ADD DSB}}$ and $\overline{\text{DO DSB}}$ must be pulled low to float the system bus.
27	PWAIT	Wait—Command/control signal out which, when high, acknowledges that processor is in Wait state.
28	PINTE	Interrupt Enable—Command/control signal out which indicates condition of Interrupt Enable flip-flop. When set (high), interrupts are accepted. Flip-flop is set by Enable Interrupt (EI) instruction. It is reset by Disable Interrupt (DI) instruction, when an interrupt is accepted, and by RESET signal.
29	A5	Address Bit 5
30	A4	Address Bit 4
31	A3	Address Bit 3
32	A15	Address Bit 15
33	A12	Address Bit 12
34	A9	Address Bit 9
35	DO1	Data Out Bit 1
36	DO0	Data Out Bit 0
37	A10	Address Bit 10
38	DO4	Data Out Bit 4

Pin No.	Signal	Definition
39	DO5	Data Out Bit 5
40	DO6	Data Out Bit 6
41	DI2	Data In Bit 2
42	DI3	Data In Bit 3
43	DI7	Data In Bit 7
44	SM1	SM1 status output signal which, when high, indicates that the current bus cycle is an op code fetch.
45	SOUT	Status output signal which, when high, indicates that the address bus contains the address of an output device and the data bus will contain the output data when $\overline{PWR}$ is active.
46	SINP	In—Status output signal which, when high, indicates that the address bus contains the address of an input device and the input data should be placed on the data bus when PDBIN is active.
47	SMEMR	Memory Read—Status output signal which, when high, indicates that the data bus will be used to read memory data.
48	SHLTA	Halt Acknowledge—Status output signal which, when high, acknowledges that a HALT instruction has been executed.
49	$\overline{CLOCK}$	Phase 2 clock inverted
50	GND	Signal and power ground
51	+8 V	Same as pin 1
52	−16 V	Negative unregulated voltage supply
53	$\overline{SSW\ DSB}$	Sense Switch Disable—A low disables the data input buffers so the input from the sense switches may be strobed onto the bidirectional data bus.
54	$\overline{EXT\ CLR}$	External Clear—A low clears I/O devices. Generated by front panel switch.
55*	RTC	Real Time Clock
	GND	Ground
56*	STSTB	Status Strobe—A low indicates that status signals are on data bus.
	DMAGR7	DMA Grant 7
	V_{CC}	Standby
57*	$\overline{DIG1}$	Data Input Gate 1
	DMAGR6	DMA Grant 6
58*	FRDY	Front Panel Ready—When low, it disables WRITE driver.
	DMAGR5	DMA Grant 5
59*	DMAGR4	DMA Grant 4
	CW	Conditioned Memory Write
	—	Memory Disable (PGANTOM)
	EXINH0	Bank Select 0
	$\overline{INH}$	Shadow Memory
	Program Switch	To enable programmer
60*	DMAGR3	DMA Grant 3
	$\overline{ABX}$	NOT Alternate Bank X (A 16)

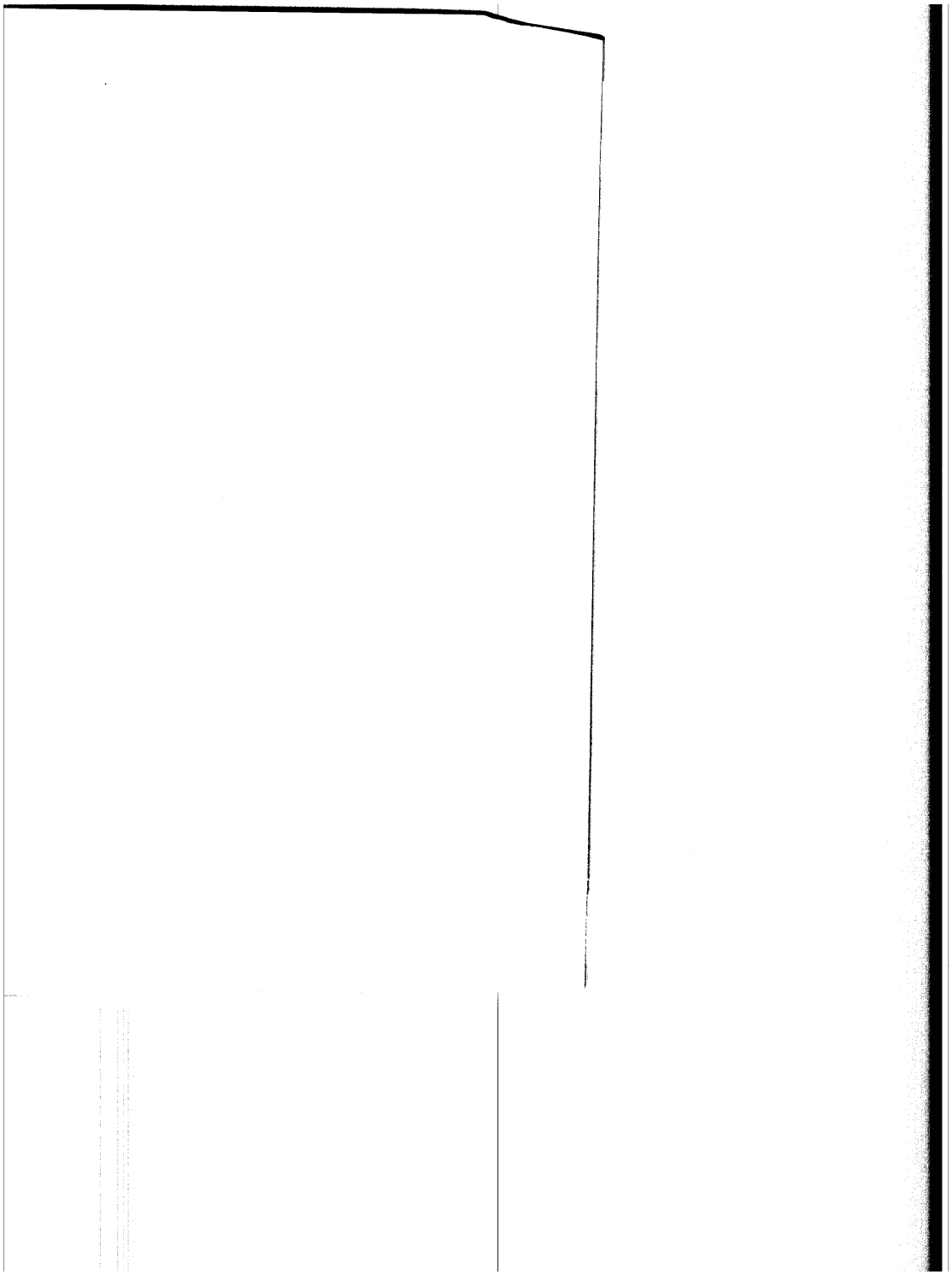
Pin No.	Signal	Definition
	MBS	Memory Bank Select
	—	Bank Select 1
	MONITOR	Enable user's monitor
61*	A17	Address line 17
	DMAGR2	DMA Grant 2
	KRDY	KIMSI Ready
	—	Bank Select 2
	GND	Ground
62*	DMAGR1	DMA Grant 1
	CK4	Phase 4 shift clock
	Kϕ2	KIMSI ϕ2 clock
	—	Bank Select 3
	A18	Address line 18
63*	DMAGR0	DMA Grant 0
	CK2	Phase 2 shift clock
	$\overline{\text{KHOLD}}$	KIMSI Hold
	—	Bank Select 4
	A19	Address Line 19
64*	$\overline{\text{DMA RCVD}}$	DMA Grant Flag
	BCE	Chip Enable
	RTC	Real Time Clock (60 Hz)
	—	Bank Select
	RDSBL/H	
65*	$\overline{\text{MREQ}}$	Memory Request
	$\overline{\text{WRITE}}$	Write Enable
	—	Bank Select 6
66*	$\overline{\text{RFSH}}$	Refrest
	LDH	Load High Address Byte
	CMCLK	Variable video clock
	—	Bank Select 7
	8/16	
67*	$\overline{\text{PHANTOM}}$	Phantom Disable—Used to disable RAM and I/O addressing
	$\overline{\text{NMI}}$	Nonmaskable Interrupt
	$\overline{\text{RFSHDSBL}}$	Refrest Disable
	$\overline{\text{MDSBL}}$	Memory Disable
	BBSY +	Phantom
	RFSH	Refrest
	SCLK	Clock (Video Sample)
	A19	Address Line 19
68	MWRITE	Memory Write—A high indicates that the current data on the Data Out Bus is to be written into the memory location currently on the address bus.
69	$\overline{\text{PS}}$	Protect Status—See pin 20.
70	PROT	Protect—See pin 20.
71	RUN	Run—A high indicates that the Run/Stop flip-flop is set to RUN on the front panel.
72	$\overline{\text{PRDY}}$	Ready—See pin 3.
73	$\overline{\text{PINT}}$	Interrupt Request—A low causes the processor to recog-

Pin No.	Signal	Definition
		nize an interrupt request at the end of the current instruction or while halted. If the CPU is in the Hold state or if the Interrupt Enable flip-flop is reset, it will not honor the request.
74	$\overline{\text{PHOLD}}$	Hold—A low requests the processor to enter the Hold state. It allows an external device to gain control of the address and data buses as soon as the current machine cycle is completed.
75	$\overline{\text{PRESET}}$	Reset—A low causes the contents of the program counter to be cleared and the instruction register is set to 0.
76	PSYNC	Sync—The command/control signal out which, when high, identifies the beginning of a machine cycle.
77	$\overline{\text{PWR}}$	Write—The command/control signal out which, when low, signifies the presence of valid data on the Data Out bus for memory write or I/O output.
78	PDBIN	Data Bus In—The command/control signal out which, when high, requests data on the DI bus from the currently addressed memory or I/O.
79	A0	Address Bit 0
80	A1	Address Bit 1
81	A2	Address Bit 2
82	A6	Address Bit 6
83	A7	Address Bit 7
84	A8	Address Bit 8
85	A13	Address Bit 13
86	A14	Address Bit 14
87	A11	Address Bit 11
88	DO2	Data Out Bit 2
89	DO3	Data Out Bit 3
90	DO7	Data Out Bit 7
91	DI4	Data In Bit 4
92	DI5	Data In Bit 5
93	DI6	Data In Bit 6
94	DI1	Data In Bit 1
95	DI0	Data In Bit 0
96	SINTA	Interrupt Acknowledge—The status output signal which, when high, identifies the instruction fetch cycle(s) that immediately follow an accepted interrupt request presented on $\overline{\text{PINT}}$.
97	$\overline{\text{SWO}}$	Write/Output—The status output signal identifying a bus cycle which, when low, transfers data from processor to memory or I/O port.
98	SSTACK	Stack—Status output signal which indicates, when high, that the address bus holds the pushdown stack address from the Stack Pointer and that a stack operation will occur on the current cycle.
99	POC	Power On Clear—Generated by PRESET or power on. Used to reset CPU and I/O devices.
100	GND	Signal and power ground.

DISCUSSION

As can be seen from the signal definitions, the S-100 bus is standardized except for those pins marked with an asterisk, pins 12–17 and 55–67. In the signal definitions column, some of the known uses for these lines have been listed; although, some new ones have probably been omitted. Some systems that are not 8080-based systems do not generate all of the signals listed. If a board requires one or more of these missing signals, then a real problem exists which may require extensive modifications.

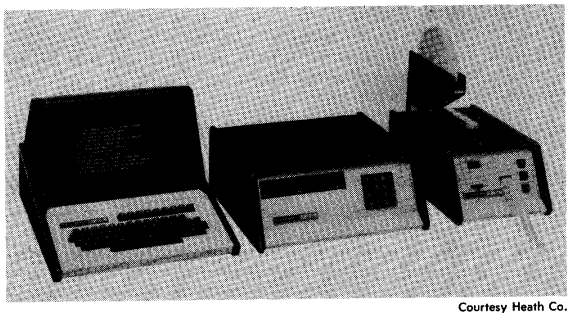
To effectively use the S-100 bus, care must be taken in reading the specifications of all boards used or contemplated being used. All boards must have the proper lines on the proper pin or capability for jumpering to the proper pin. All signals required by any of these boards must be generated somewhere in the system. Information on systems and boards may be obtained from manufacturers, computer stores, computer clubs, and other hobbyists.



CHAPTER 3

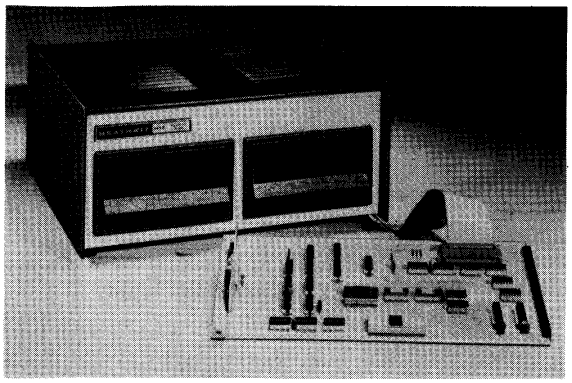
The Benton Harbor Bus

The Benton-Harbor Bus was developed by Heath Company for use on their 8080-based H8 System (shown in Fig. 3-1). Heath Company now offers the H8 System which includes the H8 (chassis, power supply, motherboard, control board, and CPU board), the H8-1 (8K × 8 memory board with 4K of memory), the H8-2 (parallel interface board), the H8-3 (4K × 8 memory for the H8-1), and the H8-5 (serial I/O and cassette interface). Heath Company also offers the H10 papertape reader/punch and the H9 video terminal (both shown in Fig. 3-1), and the H8 floppy disk (shown in Fig. 3-2). Heath Company plans to offer other boards and accessories.



Courtesy Heath Co.

Fig. 3-1. The H8 system with H9 video terminal and H10 papertape reader/punch.



Courtesy Heath Co.

Fig. 3-2. The WH17 floppy disk system.

Other companies will surely offer boards for the popular Heath system.

The approximately 5½-inch × 14⅜-inch motherboard (Fig. 3-3) is mounted vertically and has slots (P1–P10) for ten other boards to be inserted at an unusual angle. Slot P1 is reserved for the H8 control board, P2 is reserved for the H8 CPU board and slot P10 is reserved for an expansion connector. That leaves seven slots for expansion within the H8 mainframe.

A board for the Benton Harbor Bus is approximately 6 inches × 12 inches with two 25-pin connectors on one end. The connectors slide onto the pins on the motherboard. See Figs. 3-4 and 3-5 for typical boards. A bracket on the opposite end from the connectors supports the boards when they are inserted into the H8 chassis.

BENTON HARBOR BUS SIGNAL DEFINITIONS

The Benton Harbor Bus pinout designations are shown in Fig. 3-6.

Pin No.	Signal	Definitions
10–17	$\overline{D0}$–$\overline{D7}$	Data Bus—The tri-state data bus provides bidirectional communication between the CPU, memory, and I/O devices for instructions and data transfers. D0 is least significant bit. Negative true.
23	MEMW	Memory Write—A high strobes data on the data bus

1. PIN SPACING 0.1 INCH.
2. NOTE 0.2 GAP BETWEEN PINS 24 AND 25.

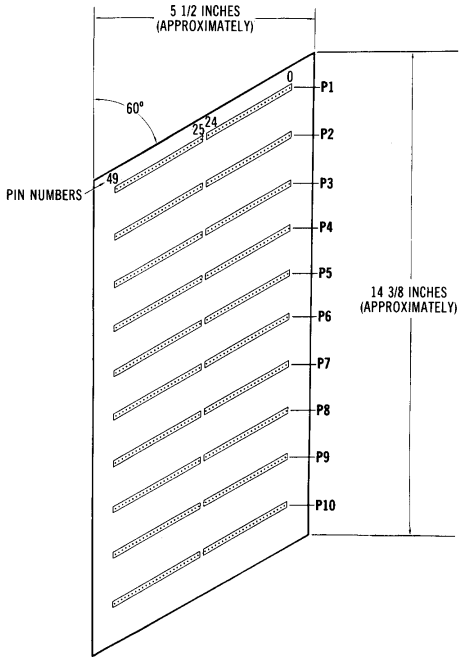
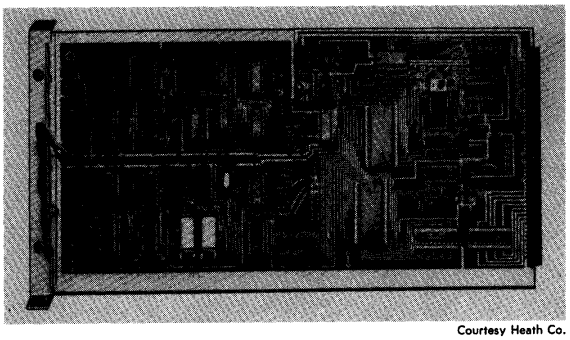


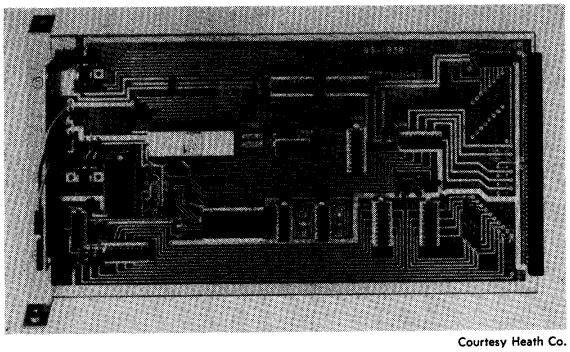
Fig. 3-3. Diagram of the Benton Harbor Bus motherboard used in the H8.

Pin No.	Signal	Definitions
		to the currently addressed memory or memory-mapped I/O devices.
21	I/OW	I/O Write—A high strobes data on the data bus to the output device currently addressed by the lower eight bits of the address bus.
28	MEMR	Memory Read—A high strobes data from the addressed memory or memory-mapped I/O device onto the data bus and into the CPU.
26	I/OR	I/O Read—A high strobes data from the addressed



Courtesy Heath Co.

Fig. 3-4. H8-5 serial I/O and cassette interface board.



Courtesy Heath Co.

Fig. 3-5. H8 CPU board.

Pin No.	Signal	Definitions
		I/O device onto the data bus and into the CPU.
30–45	$\overline{A0}$–$\overline{A15}$	Address Bus—Sixteen fully buffered lines that can select any one of 65,536 memory locations or 256 I/O ports. Negative true. A0 is least significant bit.
19	M1	Machine Cycle One—A high signifies that the machine cycle being executed is an instruction fetch.
20	$\overline{RDYIN}$*	Ready In—A low causes the processor to enter a

* Heath Company reserves the right to change these pin designations.

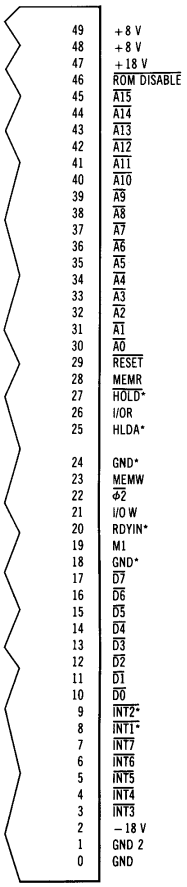


Fig. 3-6. Benton Harbor Bus pinout designations.

Pin No.	Signal	Definition
		WAIT state until pulled high again. Used by slow memory.
27	$\overline{\text{HOLD}}$*	Hold—A low causes the CPU to enter a HOLD state at the end of the current machine cycle. The address and data buses will be tri-stated allowing a DMA device to control these buses.
25	HLDA*	Hold Acknowledge—A high appears in response to the HOLD signal and indicates that the data and address buses will be tri-stated.
46	$\overline{\text{ROM DISABLE}}$	When the X1, X2 jumper on the H8 CPU board is installed, a low on this signal disables the on-board ROM allowing a test board or other ROM board to use the monitor address space.
3–7	$\overline{\text{INT}}_3$–$\overline{\text{INT}}_7$	Interrupts—A low on any combination of these lines activates the Interrupt Request of the CPU.
8, 9	$\overline{\text{INT}}_1$, $\overline{\text{INT}}_2$	Not Dedicated—The H8 CPU board has jumper pads available to jumper INT_1 and INT_2 to these bus lines in order to share the front panel interrupts, if desired. Otherwise, these lines may be used by the customer. With jumper installed, a low will activate an Interrupt Request of the CPU.
29	$\overline{\text{RESET}}$	Reset—Goes low in response to a manual reset or CPU power on. Used to put devices on bus in a known state for an orderly start up.
22	$\overline{\phi 2}$	Phase Two Clock—This buffered inverted signal is used to synchronize system devices connected to the bus.
0, 1	GND	Ground—Signal and power ground for bus.
18, 24	CPU GND	CPU Ground—These lines are grounded on the H8 CPU board but can be floated for other use by removing one jumper.
2	−18 V	−18 V—Unregulated negative supply voltage.
47	+18 V	+18 V—Unregulated positive supply voltage
48, 49	+8 V	+8 V—Unregulated positive supply voltage

DISCUSSION

Heath Company in designing the Benton Harbor Bus has stuck to the basics. Only the address bus, data bus, and generalized control lines are included. Specialized control lines are omitted so that the bus does not need to change with future alterations. A convenient design consideration on the bus is the positioning of the data bus, address bus, and interrupt lines so that the last digit of their respective number coincides with the last digit of the bus line (e.g. $\overline{\text{A6}}$ is on line 36).

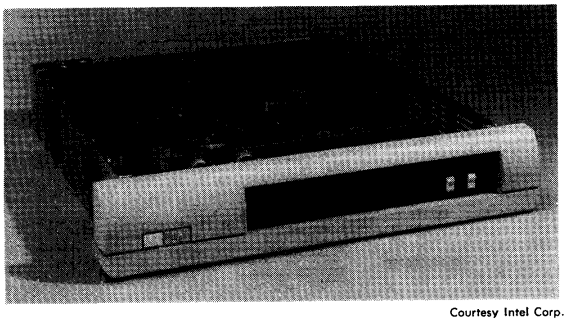
* Heath Company reserves the right to change these pin designations.

CHAPTER 4

The SBC Multibus

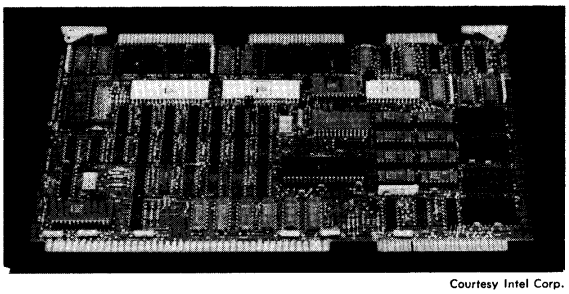
The Multibus was developed by Intel for their SBC series of boards that includes CPUs, memory, I/O, communications, high-speed math, DMA control, and others. Fig. 4-1 shows an SBC system with chassis, power supply, backplane with card cage, and CPU board. Figs. 4-2 and 4-3 show an SBC 80/20 CPU board and a combination memory and I/O expansion board, respectively. Several companies produce a wide variety of boards which will operate on the Multibus.

The SBC series is a general-purpose, inexpensive board set originally designed for OEMs so that they would not have to develop their own hardware for every new product in which they used an



Courtesy Intel Corp.

Fig. 4-1. The SBC-based 80/20 system.

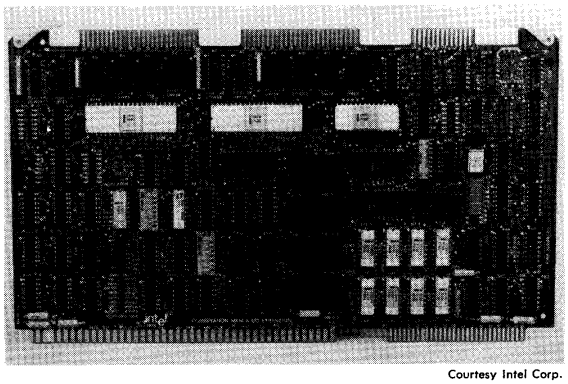


Courtesy Intel Corp.

Fig. 4-2. SBC 80/20 single-board computer.

Intel processor. The SBC system allows implementation of a tremendous variety of inputs and outputs with a small number of boards. Multimaster operation having multiplexed CPUs, DMA controllers, and disk controllers controlling the bus is easily realized.

A typical board for the Multibus is shown in Fig. 4-3. It is 12 inches long, 6.75 inches high and 0.062 inch thick with two edge connectors along the bottom as shown. (The P1 Multibus is on the left in the photo and the P2 Auxiliary Connector is on the right.) Depending on the board type, there may be up to three edge con-



Courtesy Intel Corp.

Fig. 4-3. SBC 517 combination I/O expansion board.

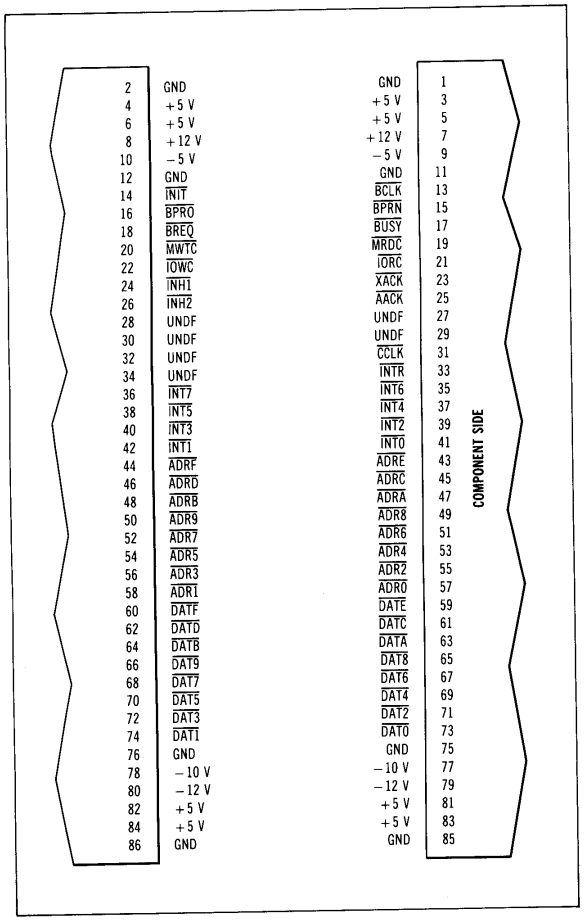


Fig. 4-4. SBC pinout designations.

nectors along the top of the board. The 86-pin P1 (Multibus) edge-connector numbers its pins from left to right as the board is viewed in Fig. 4-3. The odd pin numbers are on the component side and the even pin numbers are on the opposite side. The pinout designations are listed in Fig. 4-4.

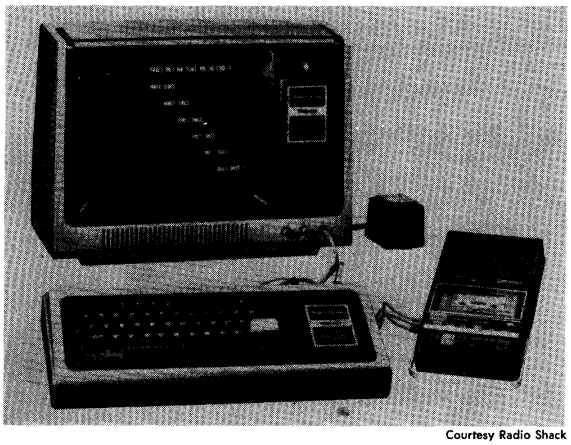
SBC SIGNAL DEFINITIONS

Pin No.	Signal	Definitions
67–74	$\overline{DAT0}$–$\overline{DAT7}$	Data Bus—Active low, bidirectional.
59–66	$\overline{DAT8}$–$\overline{DATF}$	Data Bus—For upper 8 bits in 16-bit systems.
19	$\overline{MRDC}$	Memory Read Command—A low indicates that a certain memory location is on the address bus and its contents are to be put on data bus.
20	$\overline{MWTC}$	Memory Write Command—A low indicates that a certain memory location has been addressed and data to be written into it is on the data bus.
21	$\overline{IORC}$	I/O Read Command—A low indicates that an input port has been addressed and the data at that port is to be placed on the data bus.
22	$\overline{IOWC}$	I/O Write Command—A low indicates that an output port has been addressed and that the data bus contents are to be outputted.
43–58	$\overline{ADR0}$–$\overline{ADRF}$	Address Bus—Active low address lines.
14	$\overline{INIT}$	Initialize—A low resets the entire system.
15	$\overline{BPRN}$	Bus Priority In—A low indicates that no higher priority master module is requesting use of the system bus. It is connected to signal ground in a single master system; synchronized with $\overline{BCLK}$ in a multimaster system. It is not bused on the motherboard.
16	$\overline{BPRO}$	Bus Priority Out—Connected to $\overline{BPRN}$ of master module with next lower bus priority. A low indicates to the next lower master module that a higher priority master is in control of the buses. It is not bused on motherboard.
17	$\overline{BUSY}$	Bus Busy—A low indicates that the bus is currently in use and prevents other master modules from gaining control.
18	$\overline{BREQ}$	Bus Request—A low indicates that a particular master module requires use of the bus. It is synchronized with $\overline{BCLK}$.
23	$\overline{XACK}$	Transfer Acknowledge—A low from a memory location or I/O port indicates that the specified read/write operation is complete.
25	$\overline{AACK}$	Advanced Acknowledge—A low allows memory to complete access without having the CPU wait.
33	$\overline{INTR}$	Direct Interrupt—A low from an external device generates an interrupt request.

CHAPTER 5

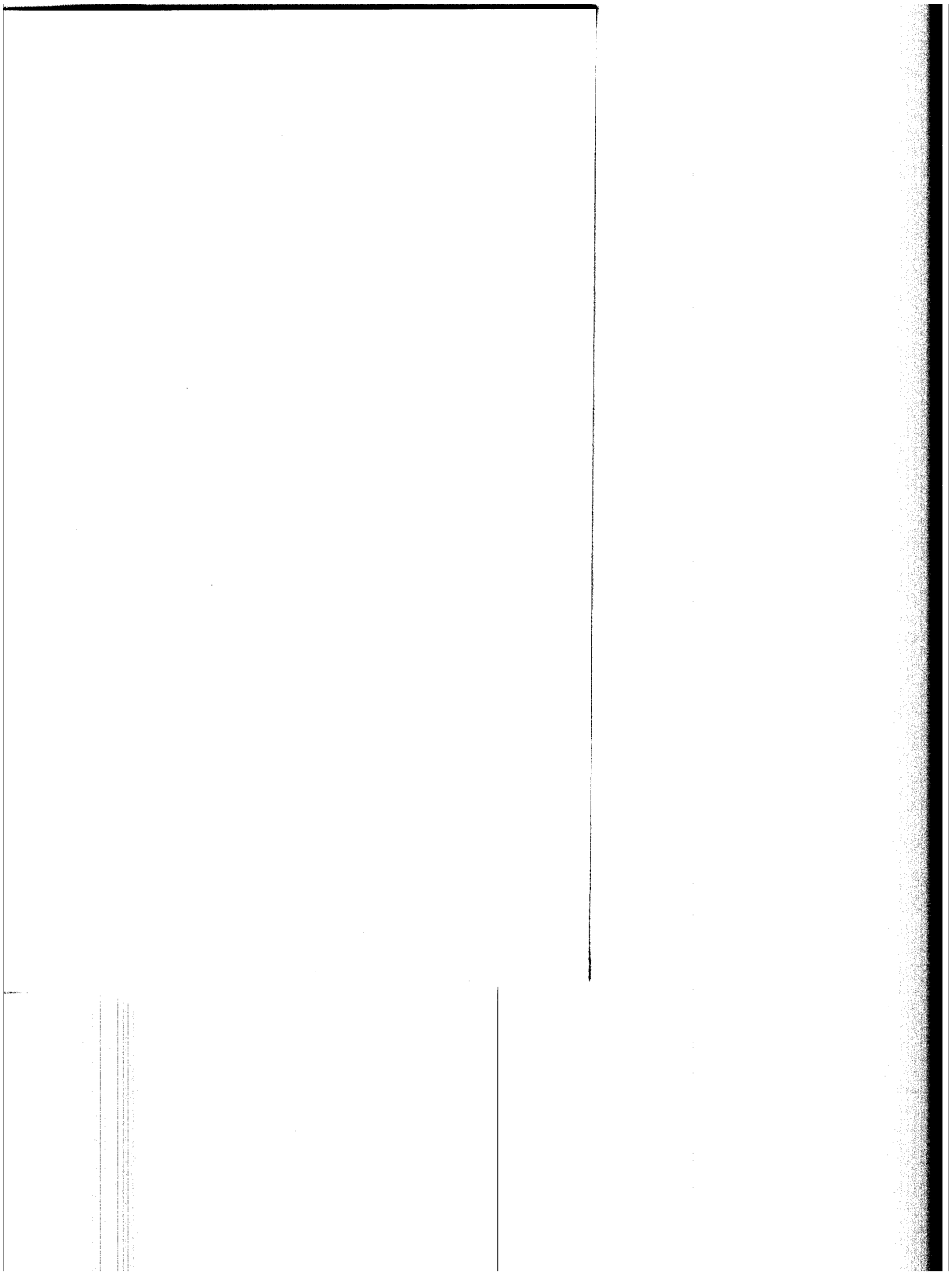
The TRS-80 Bus

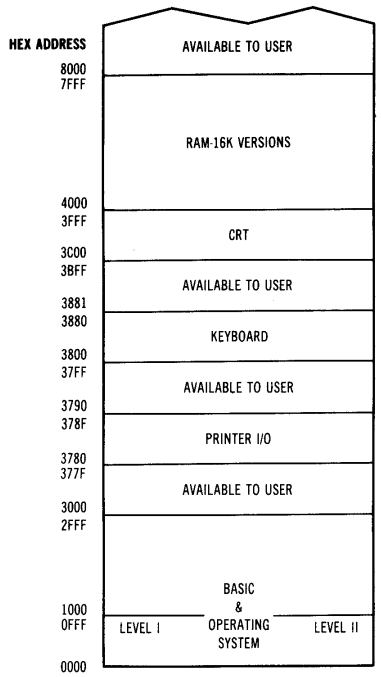
The TRS-80, shown in Fig. 5-1, is Radio Shack's very popular microcomputer system. The keyboard enclosure, shown removed in Fig. 5-2, houses the CPU, RAM, executive and BASIC ROMs, the keyboard, video and cassette interfaces, and the power supply. Floppy disk units and printers (not shown) are available to expand the system.



Courtesy Radio Shack

Fig. 5-1. The TRS-80 microcomputer system.





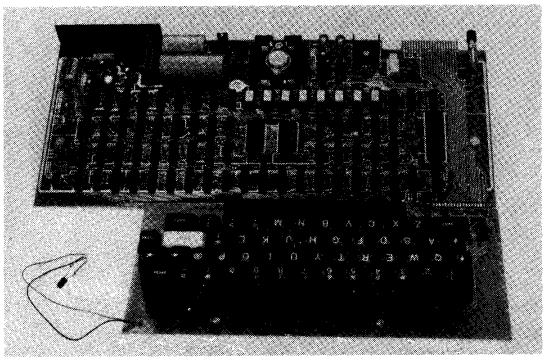
Courtesy Radio Shack

Fig. 5-4. Memory map for the TRS-80.

Because its bus is relatively straightforward, the TRS-80 is easy to expand. TRS-80 to S-100 interface boards are commercially available. The TRS-80 bus pinout designations are shown in Fig. 5-5.

TRS-80 SIGNAL DEFINITIONS

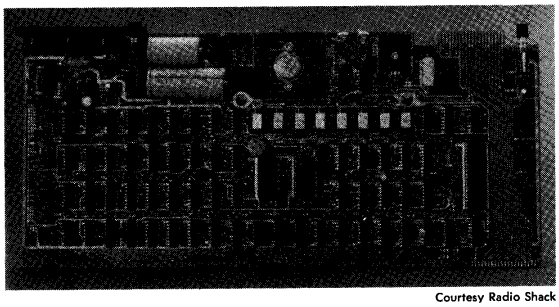
Pin No.	Signal	Definition
18, 20, 22, 24, 26, 28, 30, 32	D0–D7	Data Bus—The bidirectional data bus carries data between the processor and peripherals.



Courtesy Radio Shack

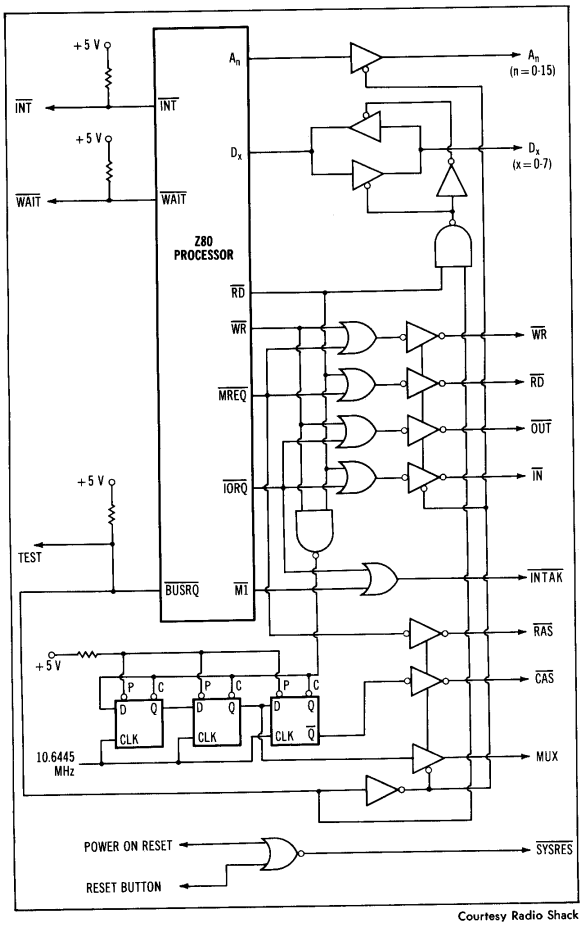
Fig. 5-2. The keyboard unit of the TRS-80 system.

Expansion of the Z80-based system is accomplished via the 40-pin (0.1-inch spacing) edge connector shown in the upper right-hand corner of Fig. 5-3. No positive indexing is provided. All lines, except as noted, are buffered. Use of dynamic RAM is simplified by address multiplex signals that are brought to the connector. The memory space above Hex 8000 is available for expansion. This is shown in the memory map given in Fig. 5-4.



Courtesy Radio Shack

Fig. 5-3. The TRS-80 board. The expansion connector is shown in the upper right-hand edge of the board.



Courtesy Radio Shack

Fig. 5-6. Diagram showing a Z80-to-bus interface.

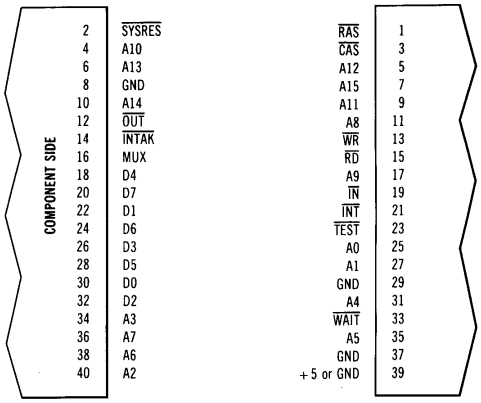


Fig. 5-5. Pinout designations for the TRS-80 bus.

Pin No.	Signal	Definition
12, 13, 15, 19	$\overline{RD}$, $\overline{WR}$, $\overline{IN}$, $\overline{OUT}$	Read, Write, Input, Output—The bus Read, Write, Input and Output lines control the memory and I/O operations. They are derived from the $\overline{Read}$, $\overline{Write}$, $\overline{Memory\ Request}$ and $\overline{I/O\ Request}$ outputs of the Z80 as shown in Fig. 5-6. The processor's Read and Write lines are active low outputs used to determine the direction of flow on the data bus. The $\overline{MREQ}$ line is an active low output used to indicate a Memory-Read or -Write operation and the $\overline{IORQ}$ line is an active low output used to indicate an input or output operation. The bus $\overline{RD}$ line is the ORed combination of the processor's Read and $\overline{MREQ}$ lines and goes low to indicate a Memory-Read operation. The bus $\overline{WR}$ line is the ORed combination of the processor's Write and $\overline{MREQ}$ lines and goes low to indicate a Memory Read. The bus $\overline{IN}$ line is an active low output that indicates an input operation, derived by ORing the $\overline{RD}$ and $\overline{IORQ}$ of the processor. The bus $\overline{OUT}$ line is an active low output that indicates an output operation, derived by ORing the processor's WR and $\overline{IORQ}$.
1, 3, 16	$\overline{RAS}$, $\overline{CAS}$, MUX	Row Address Select, Column Address Select, Address Multiplex—These lines are used in addressing industry standard 16-pin 4-kilobyte dynamic RAMs. Since only six address pins, A0–A5, are available

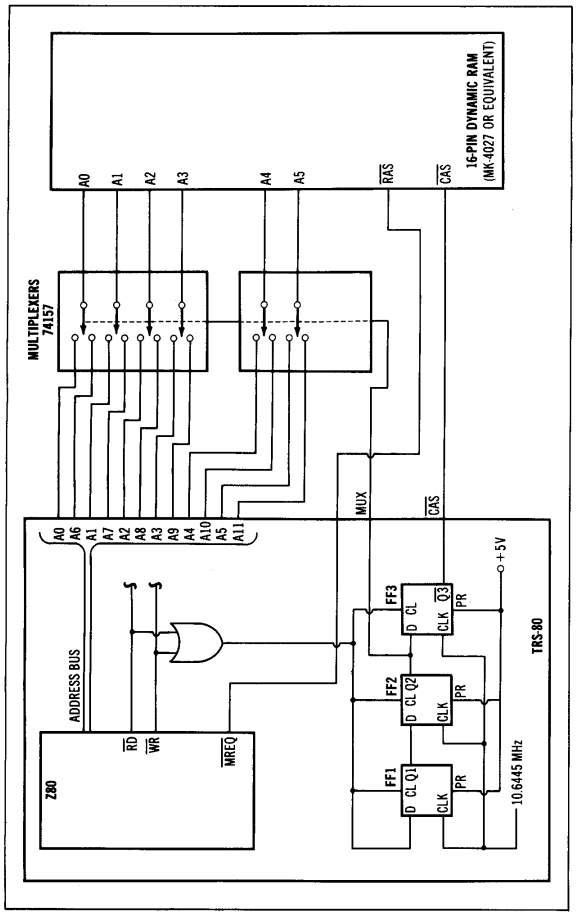


Fig. 5-7. A typical interface circuit for addressing the dynamic RAM.

on the RAM integrated circuit, the address must be fed to it in parts—multiplexed.

Internally, the RAM consists of a 64-row by 64-column array of memory cells. Any cell can be located by specifying its row address and column address. Internal circuitry can latch the row address from A0–A5 on command, and then, on command, latch the column address from the same pins to form the complete address. External circuitry must accept the address from the processor's address bus, split it into row and column halves and, then, feed it sequentially to the RAM's address lines. A typical interface circuit is shown in Fig. 5-7. All buffers and the data bus circuitry have been omitted to simplify the sketch. Address lines A0–A11 feed the data multiplexers in pairs of row and column addresses (A0 is paired with A6, etc.). Only one input of each pair is passed to the RAM at one time. The signal on the multiplex input determines which group of address inputs is selected.

At the beginning of each Read or Write cycle, the $\overline{\text{MREQ}}$ is pulled low to indicate a valid address. The $\overline{\text{MREQ}}$ is also used as the RAM row-address select signal (RAS) for the RAM which latches the signals on A0–A5. These signals are from address bus lines A0–A5.

When data is stable on D0–D7, the $\overline{\text{RD}}$ or $\overline{\text{WR}}$ line of the Z80 is pulled low. The $\overline{\text{RD}}$ and $\overline{\text{WR}}$ are inverted and ORed to feed the flip-flop chain. The clear and FF1 data inputs are controlled by the OR gate. When either the $\overline{\text{RD}}$ or $\overline{\text{WR}}$ goes low, the Clears are pulled high (inactive) and a logical 1 is loaded into flip-flop FF1 on the next 10.6445 MHz Clock pulse. The 10.6445 MHz Clock is obtained from the master system Clock which also feeds the Z80 microprocessor. The second Clock pulse transfers the logical 1 to flip-flop FF2 where it appears on output Q2. The Q2 signal is the multiplex signal (MUX) that controls the data multiplexers.

When the multiplex line goes high, the multiplexers change their outputs to reflect the A6–A11 inputs. The next Clock pulse shifts the logical 1 to flip-flop FF3. Output $\overline{\text{Q3}}$ of FF3 is the RAM column-address select signal $\overline{\text{CAS}}$, which causes the RAM to latch the A6–A11 signals now appearing on its A0–A5 inputs. The RAM now has the complete address of the desired memory cell. All of this must occur in

Pin No.	Signal	Definition
33	$\overline{\text{WAIT}}$	Wait—The Wait line is an active low input that allows the processor to work with slow memory. It is sampled each time an address is put on the bus and, if pulled low by memory or a peripheral, the processor executes Wait cycles until it is pulled high. Wait cycles delay the execution of an instruction, giving the memory or peripherals the extra time they need to access the desired data.
23	$\overline{\text{TEST}}$	Test—The Test line is an active low input used by peripherals to gain control of the external buses. It affects the processor's bus request $\overline{\text{BUSRQ}}$ input and all on-board buffers are also floated, effectively disconnecting the TRS-80 from external devices and allowing DMA-type operations.
39	+5 V, GND	This power line is a 5 V dc output on level I computers and a system ground on level II computers.
8, 29, 37	GND	Ground—The ground line is a common return for all system power supplies and signals.

Pin No.	Signal	Definition
		a short period of time since the RAM must make available, or be able to accept, data from the bus while $\overline{RD}$ or $\overline{WR}$ is low. When $\overline{RD}$ or $\overline{WR}$ goes high, the flip-flop Clear lines are pulled low clearing them and resetting the multiplexers to reflect the Z80 A0–A5 lines.
2	$\overline{SYSRES}$	System Reset—The system Reset line is the output of an internal Reset circuit. It is pulled low during power up or when the Reset button is pushed and it can be used to reset peripherals.
4–7, 9–11, 17, 25, 27, 31, 34–36, 38, 40	A0–A15	Address Bus—The address bus lines output the location of the byte desired by the processor.
21	$\overline{INT}$	Interrupt Request—The Interrupt Request input feeds $\overline{INT}$ of the Z80. When pulled low, the processor finishes the current instruction and examines the "I" flip-flop. If it is set, the processor pushes the program counter on the stack, resets the "I" flip-flop and begins the Interrupt Service routine. The processor's response to an Interrupt is software selectable to one of three modes. In Mode 0, the processor pulls $\overline{INTAK}$ low and expects the interrupting peripheral to place the instruction to be executed next on the data bus. In Mode 1, the processor loads the program counter with Hex 0066 and begins execution. In Mode 2, the processor loads the program counter with the contents of two contiguous locations which are pointed to by the combination of the I register contents and an address supplied on the data bus by the interrupting device. In Modes 1 and 2, the user must, obviously, have the service routine at the proper locations. If the "I" flip-flop is reset when an Interrupt Request occurs, the processor will ignore the request until the flip-flop is set.
14	$\overline{INTAK}$	Interrupt Acknowledge—The Interrupt Acknowledge line is a derived output that is pulled low at the beginning of an Interrupt service routine. It indicates in Modes 0 and 2 that the device requesting service should place a byte on the data bus. It is derived by ORing the processor's $\overline{IORQ}$ and $\overline{M1}$ output lines, which go low simultaneously to indicate an Interrupt service is beginning.

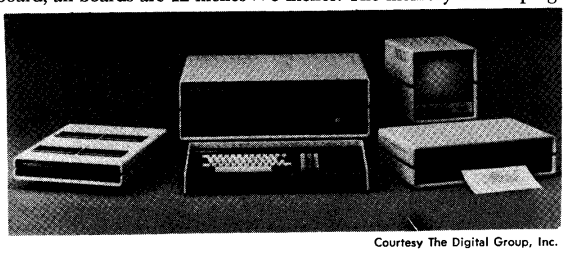
CHAPTER 6

The Digital Group Bus

The bus philosophy used in The Digital Group microcomputers, shown in Fig. 6-1, provides for the use of almost any microprocessor chip. A nearly complete set of lines allows operation with an 8080, a Z80, and a 6800 or 6502 processor board. The data lines are separated into memory input, memory output, peripheral input and peripheral output lines. The address lines are duplicated in memory and peripheral address lines. Interrupt and DMA capabilities are included.

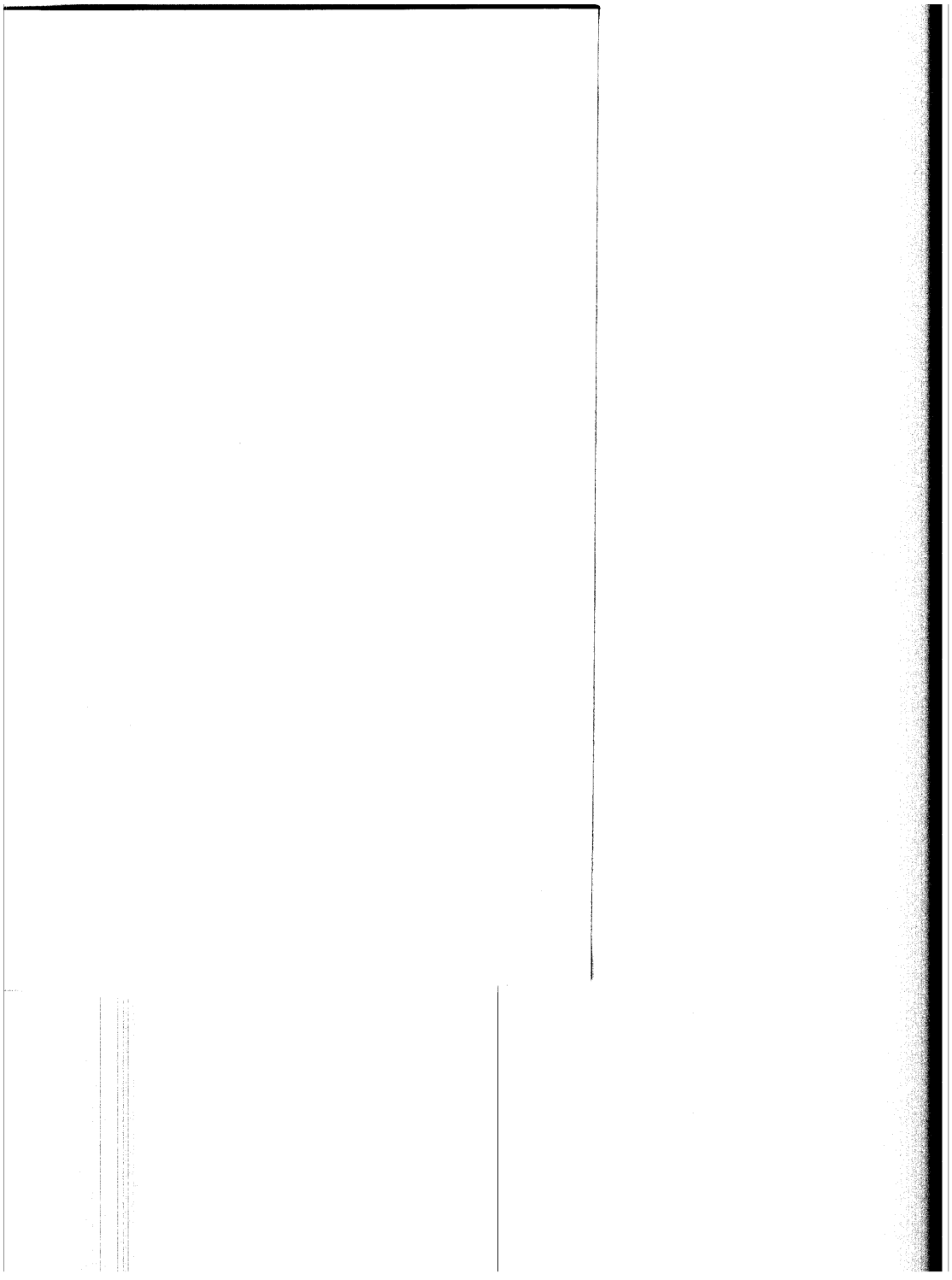
A standard motherboard from The Digital Group, Inc., shown in Fig. 6-2, has connectors for three memory boards, a processor board, a dedicated I/O board, a video terminal board, and three general-purpose I/O boards. This is more clearly seen by the view of the bare motherboard shown in Fig. 6-3.

Although four different type connectors are used on the motherboard, all boards are 12 inches × 5 inches. The memory boards plug

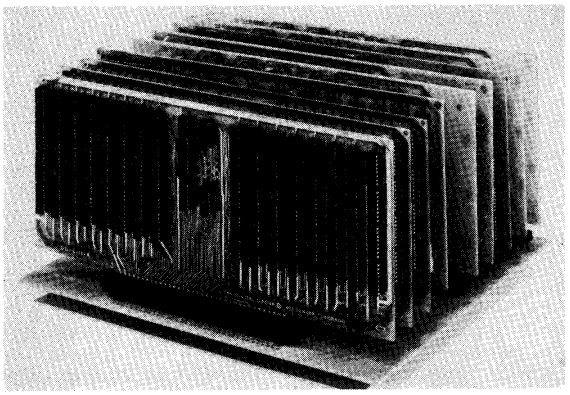


Courtesy The Digital Group, Inc.

Fig. 6-1. A microcomputer by The Digital Group, Inc.

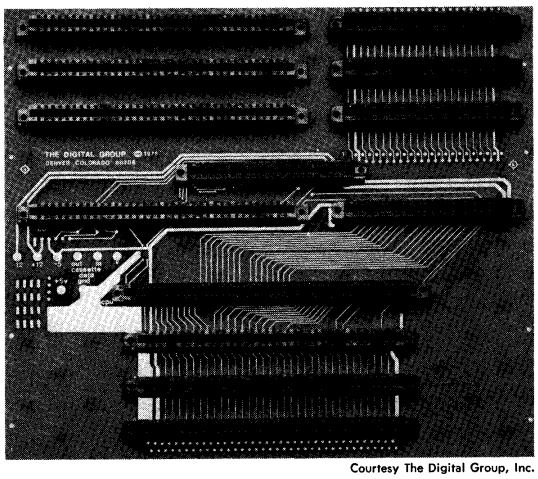


Pin No.	Signal	Definitions
35–42	$\overline{\text{INT0}}$–$\overline{\text{INT7}}$	Parallel Interrupt Requests—A low from an external device generates an interrupt request.
13	$\overline{\text{BCLK}}$	Bus Clock—Used to synchronize bus control circuits on all master modules. It may be slowed, stopped, or single stepped.
31	$\overline{\text{CCLK}}$	Constant Clock—Provides a clock signal of constant frequency for use by optional memory and I/O boards.
1, 2, 11, 12, 75, 76, 85, 86	GND	Signal ground
3–6, 81–84	+5 V	+5 V dc regulated voltage
7, 8	+12 V	+12 V dc regulated voltage
9, 10	−5 V	−5 V dc regulated voltage
79, 80	−12 V	−12 V—A −12 V dc regulated.
24	$\overline{\text{INH1}}$	Inhibit 1—Disables RAM memory devices. Allows ROM to override RAM in same address.
26	$\overline{\text{INH2}}$	Inhibit 2—Disables ROM memory devices. Allows auxiliary ROM to override ROM in same address.
27–30, 32, 34	UNDF	Undefined—These lines are undefined on the bus.
77, 78	−10 V	−10 V—A −10 V dc (for MDS 800 compatibility).



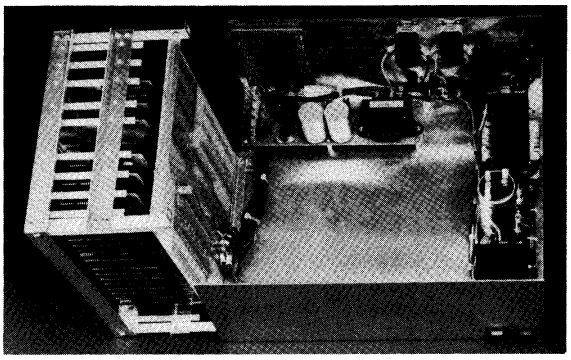
Courtesy The Digital Group, Inc.

Fig. 6-2. A populated motherboard.



Courtesy The Digital Group, Inc.

Fig. 6-3. The Digital Group's standard motherboard.



Courtesy The Digital Group, Inc.

Fig. 6-4. An open system by The Digital Group, Inc.

into 86-pin (43 on each side) double-sided edge-card connectors. The connectors have a 0.156-inch spacing. The processor board plugs into a 100-pin, 0.1-inch, double-sided, edge-card connector. The video board plugs into a 44-pin, 0.156-inch, double-sided, edge-card connector.

Each I/O card has two connectors. The I/O bus signals are brought to a 44-pin, 0.156-inch, double-sided edge-card connector. A 72-pin, 0.156-inch, double-sided edge-card connector is also provided to serve as the connection points for input and output lines. The lines on these connectors are not bused or wired to any other connector on the motherboard. They serve only the ports on the board with which they are associated. Fig. 6-4 shows an open system with the motherboard swung out. Notice the absence of runs to the 72-pin I/O connectors on the lower right side of the motherboard. Positive indexing is not provided for any of the connectors.

External connections to the I/O boards are made through the backplane board mounted in the left side of the back panel shown in Fig. 6-4. Although none are shown, wires join the backplane connectors and the 72-pin I/O connectors on the motherboard. Two 22-pin, double-sided, edge-card connectors are available to the user as well as connectors specified for keyboard, disk, printer and digital cassette deck. Additional user I/O connectors can be mounted in holes provided in the back panel. Since system expansion can be accomplished using either the memory or I/O slots, both will be examined.

MEMORY BUS SIGNAL DEFINITIONS

The memory-connector pinout designations are shown in Fig. 6-5.

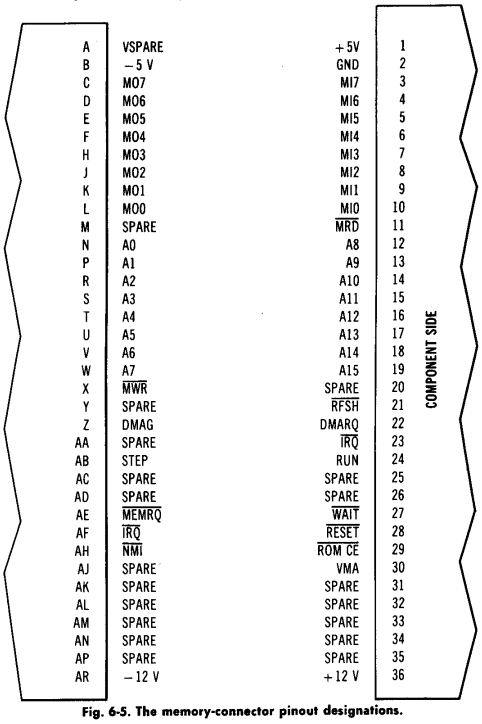


Fig. 6-5. The memory-connector pinout designations.

Pin No.	Signal	Definition
3–10	MI0–MI7	Memory Input—The memory input lines carry data from memory to the processor's D0–D7 data lines.
11	$\overline{\text{MRD}}$	Memory Read—The memory-read data strobe is an active low control line that is pulled low by the processor to transfer the data on the memory input lines.

Pin No.	Signal	Definition
L, K, J, H, F, E, D, C	MO0–MO7	Memory Output—The memory output lines carry data from the processor's D0–D7 data lines to memory.
X	$\overline{\text{MWR}}$	Memory Write—The memory-write data strobe is an active low control line that is pulled low by the processor to transfer data on the memory-output lines.
27	$\overline{\text{WAIT}}$	Wait Request—The wait line is an active low input to the processor board. It is used by slow memory to gain more time to set up or retrieve data from the memory input or output lines.
12–19, N, P, R, S, T, U, V, W	A0–A15	Memory Address—The memory address lines are the buffered outputs of the address lines of the processor and carry the number of the desired location to memory.
30	VMA	Valid Memory Address—The VMA is a processor output that indicates a stable, valid address on the address lines. It is available only in 6800-based systems. In other systems, this line is undefined.
AE	$\overline{\text{MRQ}}$	Memory Request—The memory request is an active low processor output that is pulled low to indicate a memory operation in Z80-based systems. It is undefined in configurations using other processors.
29	$\overline{\text{ROM CE}}$	ROM Chip Enable—The $\overline{\text{ROM CE}}$ is an active low output used to enable a bootstrap cassette loader ROM placed in Hex locations 0000 to 00FF. The bootstrap ROM would normally be used only during system power up. This line is controlled by an external switch and allows the user to gain those 256 bytes of memory space for RAM use after the loader has been used.
21	$\overline{\text{RFSH}}$	Refresh—The refresh line is an active low output of the Z80 during an op code fetch M1 cycle. It indicates to dynamic RAM refresh circuitry that address lines A0–A6 contain the next refresh row address. The refresh circuitry can then perform the refresh function without slowing the processor.
28	$\overline{\text{RESET}}$	Reset—This line is an active low input to the processor's reset line. Pulling it low will always reinitialize the system.
AH	$\overline{\text{NMI}}$	Nonmaskable Interrupt—The $\overline{\text{NMI}}$ is an active low input to the processor's $\overline{\text{NMI}}$ line in Z80-, 6800- and 6502-based systems. Pulling it low generates an interrupt request that must be serviced by the processor.
23, AF	$\overline{\text{IRQ}}$	Interrupt Request—The $\overline{\text{IRQ}}$ is an active low input to the processor's $\overline{\text{IRQ}}$ line. Pulling it low causes the processor to check the interrupt status bit and, if not masked, service the request. The "I" status bit is under software control and can be masked to prevent the processor from servicing the request.

Pin No.	Signal	Definition
24	RUN	Run—The Run line is an input that can stop or single step the processor through its $\overline{\text{WAIT}}$ line when used with the Stop/Step input. It must be pulled high to allow normal execution.
AB	STEP	Step—The STEP/STOP line is an input that is used to single step execution of a program when the processor has been stopped by the RUN line. Pulling this line to +5 V will single step the processor allowing close inspection of execution through front-panel indicators.
22, Z	DMARQ, DMAG	Direct Memory Access Request and Grant—The DMARQ input is used by peripherals to gain control of the buses. When pulled high by a peripheral, the processor stops execution and puts its address, data out, $\overline{\text{MEM RD}}$, $\overline{\text{MEM WR}}$, $\overline{\text{MEM RQ}}$ and $\overline{\text{RFSH}}$ buffers in a high impedance state. The DMAG line is pulled high to indicate that the lines are floating and the DMA operation can begin.
20, 25, 26, 31–35, M, Y, AA, AC, AD, AJ–AP	SPARE	Spare—These lines are not dedicated and can be user defined.
1	+5 V	+5 V—This power supply line provides filtered, regulated voltages.
B	−5 V	−5 V—This power-supply line provides filtered, regulated voltages.
36	+12 V	+12 V—This power-supply line provides filtered, regulated voltages.
AR	−12 V	−12 V—This power-supply line provides filtered, regulated voltages.
A	VSPARE	Spare Voltage—The Vspare is reserved for an additional but yet undefined power line.
2	GND	Ground—The ground line is the common system power-supply and signal-line return.

I/O SIGNAL DEFINITIONS

The signals available at the I/O connectors are a limited subset of the lines of the processor. They allow use of most parallel and serial interface chips. Memory expansion should occur through the memory connectors. The I/O pinout designations are shown in Fig. 6-6.

Pin No.	Signal	Definition
3–10	PI0–PI7	Peripheral Input—The peripheral input lines carry the complement of data from peripherals to the processor's

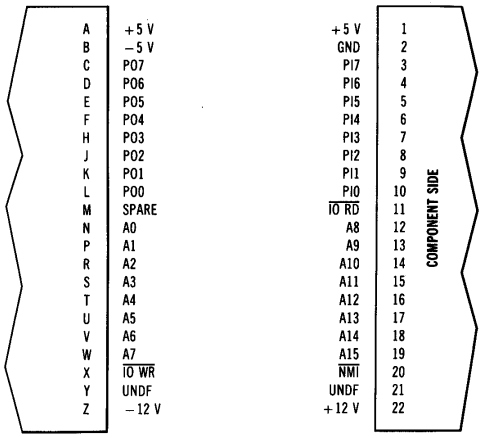


Fig. 6-6. I/O pinout designations.

Pin No.	Signal	Definition
		D0–D7 data lines through inverting buffers. The inverters can be replaced to transfer noninverted data.
11	$\overline{\text{IO RD}}$	Input/Output Read—The I/O read strobe is an active low control line that is pulled low by the processor to transfer data on the peripheral input lines.
C, D, E, F, H, J, K, L	PO0–PO7	Peripheral Output—The peripheral output lines carry data from the processor's D0–D7 data lines to peripherals. These lines are not inverted.
X	$\overline{\text{IO WR}}$	Input/Output Write—The I/O write strobe is an active low control line, pulled low by the processor, to transfer data on the peripheral output lines.
12–19, N, P, R, S, T, U, V, W	A0–A15	Peripheral Address—The peripheral address lines carry the desired I/O port location from the processor to peripherals. Only A0–A7 are active in Z80- and 8080-based systems.
20	$\overline{\text{NMI}}$	Nonmaskable Interrupt—The $\overline{\text{NMI}}$ is an active low input to the processor's $\overline{\text{NMI}}$ line on Z80-, 6800- and 6502-based systems. When pulled low, the processor must service the request.
21, Y	UNDF	CPU–I/O Undefined—These lines are reserved for processor–I/O signals but are not yet defined.
M	SPARE	Spare—The spare is an unspecified undefined line available to the user.

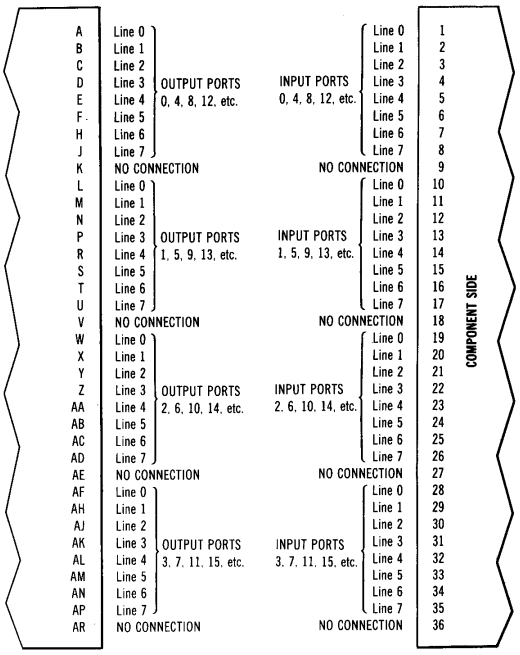


Fig. 6-7. Suggested peripheral pin designations.

Pin No.	Signal	Definition
1, A, B, 22, Z	+5 V, −5 V, +12 V, −12 V	+5 V, −5 V, +12 V, −12 V—These power-supply lines provide filtered, regulated voltages.

DISCUSSION

The 72-pin I/O connector is not connected to any internal lines but provides convenient connection from external devices to on-board peripheral circuitry. Suggested port- and line-number designations of these unconnected pins are given in Fig. 6-7.

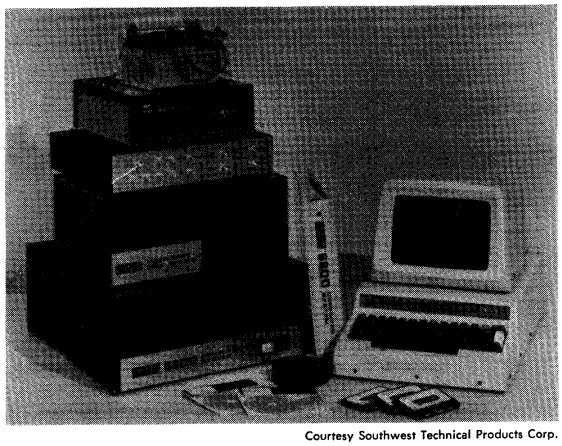
CHAPTER 7

The SS-50 Bus

The SS-50 bus was introduced in 1975 by Southwest Technical Products Corporation (SWTPC) for their SWTPC 6800 microcomputer system. Figs. 7-1 and 7-2 show the system. Since then, use of the SS-50 has grown so that, today, at least a dozen manufacturers produce components for it that range from disk controllers to digital video boards. All manufacturers of the SS-50 conform to the original bus definitions laid down by Southwest Technical Products Corporation. The compatibility problems that plague the S-100 bus do not exist for the SS-50 bus.

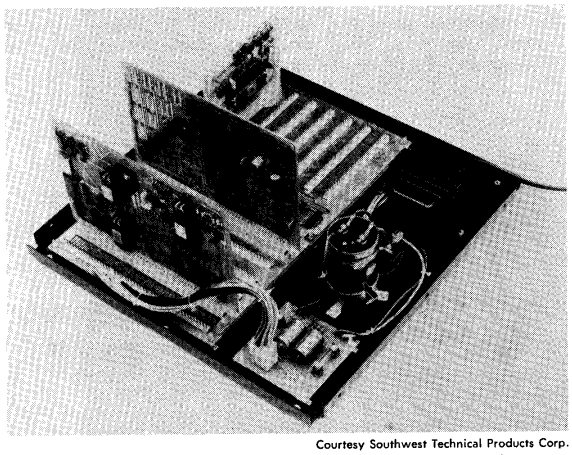
Courtesy Southwest Technical Products Corp.

Fig. 7-1. The SWTPC 6800 microcomputer.



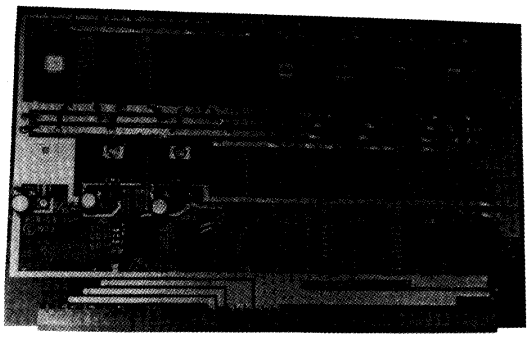
Courtesy Southwest Technical Products Corp.

Fig. 7-2. A complete SS-50 system.



Courtesy Southwest Technical Products Corp.

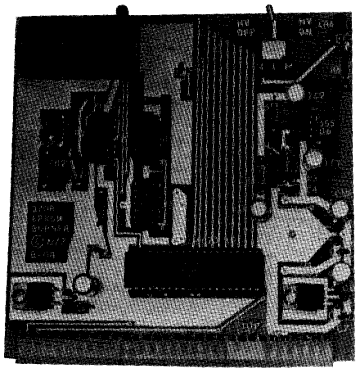
Fig. 7-3. The SWTPC 6800 motherboard showing SS-50 and SS-30 boards.



Courtesy The Micro Works

Fig. 7-4. An SS-50 PROM board.

Since it was based on the SWTPC 6800 microcomputer system, the SS-50 bus easily supports the 6800 and 6502 processors. Unlike the 8080, these processors do not multiplex control signals on the data bus. All control signals are derived on the processor. Parallel and serial I/O ports and memory are all treated alike by the CPU. Each is addressable and must respond to a simple R/W line and the address bus.



Courtesy The Micro Works

Fig. 7-5. An SS-30 EPROM programmer board.

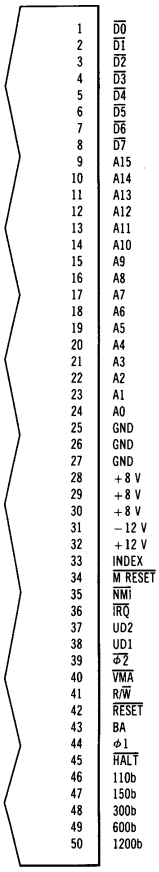
Most of the signals on the SS-50 bus come directly from the 6800 processor. The SS-50 data bus is bidirectional; it is not split into data-in and data-out lines.

The SWTPC motherboard, shown in Fig. 7-3, accepts two different size boards—an SS-50 board (shown in Fig. 7-4) and a peripheral board called the SS-30 (shown in Fig. 7-5). The SS-30 board uses a subset of SS-50 signals. Each board will be discussed in turn.

SS-50 SIGNAL DEFINITIONS

The SS-50 boards are 9 inches × 5½ inches in size. They plug into the motherboard through 50-pin Molex connectors as shown in Figs. 7-3 and 7-4. The pins are numbered from right to left. Positive indexing is provided by plugging Pin 33 on all boards. The SS-50 pinout designations are listed in Fig. 7-6.

Pin No.	Signal	Definition
1–8	D0–D7	Data Bus—The SS-50 data bus is the complement of the 6800 data-bus lines D0–D7. These lines are bidirectional and carry information between the processor and all peripherals.
41	R/$\overline{W}$	Read/Write—The read/write line of the processor, connecting the processor and peripherals, determines the direction of data flow on data-bus lines D0–D7. When it is high, data flows into the processor in a Read operation. When it is low, data flows out of the processor in a Write operation.
9–24	A0–A15	Address Lines—The address-bus lines of the processor connect the processor and peripherals, thereby providing the desired address.
40	$\overline{VMA}$	Valid Memory Address—This valid memory-address line is the complemented 6800 VMA line. It goes low when a valid address has been placed on the address bus. It is often used to enable peripherals.
34	$\overline{M\ RESET}$	Manual Reset—The manual reset line is the input to a one-shot multivibrator. When pulled low by pressing the reset button, the one-shot develops a pulse on the reset line which resets the system.
42	$\overline{Reset}$	Reset—The reset line is the output of the one-shot triggered either by the M RESET or automatically on system power up. It is connected to the reset input of the processor, and to other resettable peripherals. The processor responds to this line by loading the program counter with the contents of the reset vector and beginning execution.
35	$\overline{NMI}$	Nonmaskable Interrupt—The nonmaskable interrupt is an active low line connected to the processor's NMI input. The processor responds to this line by halting execution



1	$\overline{D0}$
2	$\overline{D1}$
3	$\overline{D2}$
4	$\overline{D3}$
5	$\overline{D4}$
6	$\overline{D5}$
7	$\overline{D6}$
8	$\overline{D7}$
9	A15
10	A14
11	A13
12	A12
13	A11
14	A10
15	A9
16	A8
17	A7
18	A6
19	A5
20	A4
21	A3
22	A2
23	A1
24	A0
25	GND
26	GND
27	GND
28	+8 V
29	+8 V
30	+8 V
31	−12 V
32	+12 V
33	INDEX
34	$\overline{M\ RESET}$
35	$\overline{NMi}$
36	$\overline{IRQ}$
37	UD2
38	UD1
39	$\overline{\phi 2}$
40	$\overline{VMA}$
41	$R/\overline{W}$
42	$\overline{RESET}$
43	BA
44	$\phi 1$
45	$\overline{HALT}$
46	110b
47	150b
48	300b
49	600b
50	1200b

Fig. 7-6. The S5-50 pinout designations.

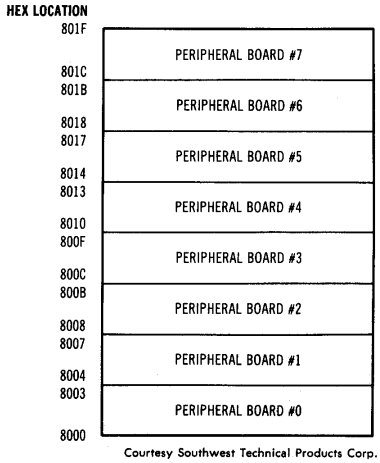
Pin No.	Signal	Definition
		of the current program, storing the vital registers on the stack, loading the program counter with the contents of the NMI vector and beginning execution of the NMI service routine. The processor must respond to an input on this line.
36	$\overline{IRQ}$	Interrupt Request—This is an active low line connected to the processor's IRQ input. The processor can, if the interrupt status flag is set, ignore an input on this line. If the "I" flag is reset, it can respond to an input by halting execution of the current program, storing the vital registers on the stack, loading the program counter with the contents of the IRQ vector and beginning execution of the IRQ service routine.
45	$\overline{HALT}$	Halt—The Halt is an active low line connected to the halt input of the processor. The processor responds to this line by halting execution of the current program and floating the address and data buses and the R/W line. An external device may then access memory for DMA or other peripherals.
43	BA	Bus Available—This is an output connected to the BA line of the processor. Although normally low, it goes high in response to a Halt input signalling an external device that the buses are available for DMA.
44	$\phi 1$	$\phi 1$—The $\phi 1$ line is the $\phi 1$ output from the two-phase nonoverlapping clock of the processor.
39	$\overline{\phi 2}$	$\overline{\phi 2}$—The $\overline{\phi 2}$ output is an inverted $\phi 2$ output from the processor's two-phase nonoverlapping clock and is used to indicate the presence of valid data on the data bus.
37, 38	UD1, UD2	User Defined—User defined lines 1 and 2 are common to all SS-50 boards but are not assigned functions. They allow the user to customize by assigning them special functions in his system.
46–50	110b, 150b, 300b, 600b, 1200b	Serial Clock—The serial clock lines are the outputs of a crystal-controlled baud-rate generator and can be used by a serial interface peripheral.
25–27	GND	Ground—The ground line is the common return line for all of the system power supplies.
28–30	+8 V	+8 Volt—The +8-volt line is an unregulated power-bus input that can be used by on-board regulators to develop +5 volts.
31	−12 V	−12 Volt—The −12-volt line is a regulated negative 12-volt input.
32	+12 V	+12 Volt—The +12-volt line is a regulated positive 12-volt input.
33	INDEX	Index—The index line is physically plugged to prevent incorrect insertion of a system board.

DISCUSSION

The advent of the 6809 processor chip, capable of two byte instructions, will bring changes to the SS-50. The baud-rate lines will be reassigned with baud-rate generation becoming the responsibility of the serial peripheral interface board. The $\phi 1$ line will be reassigned as the slow memory signal line. However, many of the lines will remain unchanged, including the user defined lines.

THE SS-30 PERIPHERAL BOARD

The SS-30 is a subset of SS-50 signals designed to facilitate use of both serial and parallel interface devices. The most obvious difference between the two is the absence of the address bus on the SS-30. It is replaced by board select lines which are derived from the SS-50 address bus. The SWTPC 6800 motherboard accommodates eight peripheral boards on the SS-30. Each board has been assigned a block of four contiguous addresses in memory as shown in Fig. 7-7. Address decoding circuitry on the motherboard generates a board select signal (using a 1-of-8 decoder) when the base address assigned a board is put on the address bus. Since the SWTPC



Courtesy Southwest Technical Products Corp.

Figs. 7-7. Memory locations of the SS-30 interface boards.

motherboard can accommodate eight peripheral boards, there are eight board select lines. The board select signal is fed only to the proper board which must then respond to the register select lines, RS0 and RS1. The RS0 and RS1 lines are connected to all peripheral boards and represent address bus lines A0 and A1. Using the RS0 and RS1 lines, a board can determine which of its four locations is being addressed. One of the peripheral boards is usually dedicated to serial communications with an external terminal. SS-30 boards are 5 inches × 4 inches and plug into the motherboard through 30-pin connectors as shown in Figs. 7-3 and 7-5. Positive indexing is provided by plugging Pin 7.

SS-30 SIGNAL DEFINITIONS

The SS-30 pinout designations are listed in Fig. 7-8.

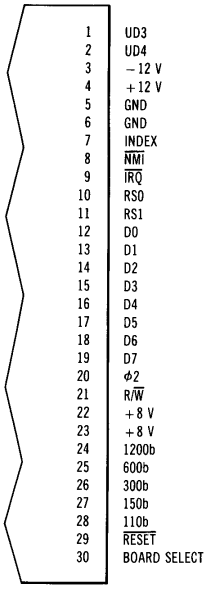
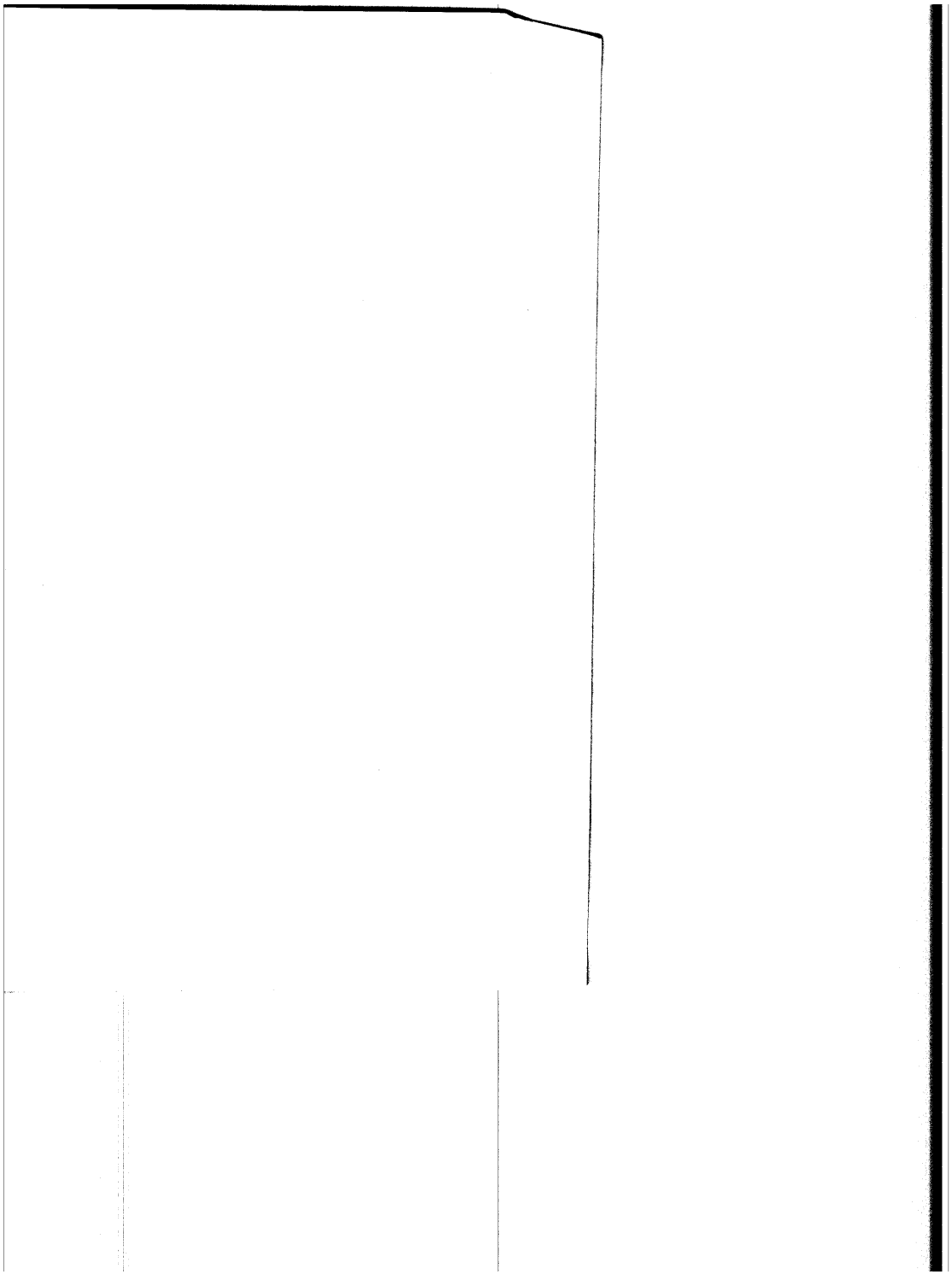


Fig. 7-8. The SS-30 pinout designations.

Pin No.	Signal	Definition
1, 2	UD3, UD4	User Defined 3 and 4—These lines are common to all the SS-30 boards but not assigned functions. They are available to the user to allow special individualized functions. They are not connected to UD1 and UD2 on the SS-50.
3, 4	−12 V, +12 V	±12 Volt—The ±12-volt supply from the SS-50.
5, 6	GND	Ground—The ground line from the SS-50.
7	INDEX	Index—The index line is physically plugged to prevent incorrect insertion of a peripheral board.
8, 9	$\overline{\text{NMI}}$, $\overline{\text{IRQ}}$	Nonmaskable Interrupt and Interrupt Request—These are the nonmaskable interrupt and interrupt request lines from the SS-50.
10, 11	RS0, RS1	Register Select—Register select lines 1 and 2 are connected to the SS-50 address-bus lines A0 and A1, respectively. They are used by a peripheral board (when signalled by its board select line) to determine which of its four addresses is being accessed.
12–19	D0–D7	Data Lines—Data lines D0–D7 are inverted $\overline{\text{D0}}$–$\overline{\text{D7}}$ lines from the SS-50.
20	$\phi 2$	$\phi 2$—The $\phi 2$ line is the inverted $\overline{\phi 2}$ line from the SS-50.
21	R/$\overline{\text{W}}$	Read/Write—This is the Read/Write line from the SS-50.
22, 23	+8 V	+8 Volt—This is the +8-volt unregulated supply from the SS-50.
24–28	1200b, 600b, 300b, 150b, 110b	Serial Clock—These are the serial clock lines from the SS-50.
29	$\overline{\text{RESET}}$	Reset—This is the RESET line from the SS-50.
30	$\overline{\text{BOARD SELECT}}$	Board Select—There are eight board select lines, one to each peripheral board. The select lines are active low. Thus, the board line selected is low while the others are held high. Only one board can be selected at a time. The board select lines are decoded from the SS-50 address bus. The address of each board follows:

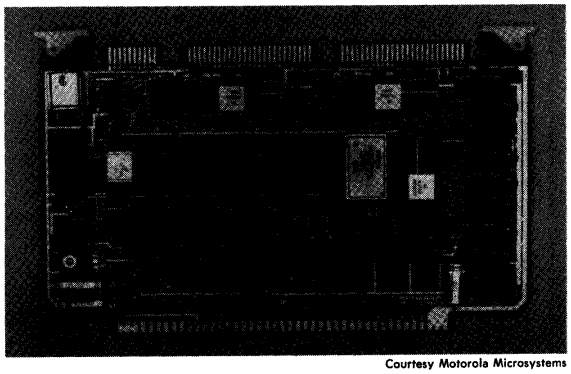
Board and Line Number	Lowest Hex Address
SEL 0	8000
SEL 1	8004
SEL 2	8008
SEL 3	800C
SEL 4	8010
SEL 5	8014
SEL 6	8018
SEL 7	801C



CHAPTER 8

The Exorcisor Bus

Motorola introduced the Exorcisor as a system development and debugging aid for their 6800 microprocessor and its family of support chips. It is widely used in industry and has grown in popularity among hobbyists. A wide variety of system configurations are available ranging from single-board computers, like the 68MM 01A shown in Fig. 8-1, to expanded disk-based systems. The TTY-based EVKI and Hex keypad and display-based EVKII (shown unassembled in Fig. 8-2) have been popular hobbyist systems. Over



Courtesy Motorola Microsystems

Fig. 8-1. An Exorcisor-compatible micromodule system.

20 companies produce Exorcisor compatible boards, of which, most are data conversion boards.

Exorcisor boards are 5¾ inches × 9¾ inches. They use an 86-pin (43 on each side) edge connector as shown in Fig. 8-1. No positive indexing is provided on all system boards.

Courtesy Motorola Microsystems

Fig. 8-2. Motorola's 6800 Evaluation Kit II.

EXORCISOR BUS SIGNAL DEFINITIONS

The Exorcisor bus pinout designations are shown in Fig. 8-3.

Pin No.	Signal	Definition
29–32, H, J, K, L	$\overline{D0}$–$\overline{D7}$	Data Bus—The bidirectional data-bus lines over which data passes between the processor and the peripherals.
6	R/W	Read/Write—The read/write lines are an output from the processor that informs peripherals of the direction of data transfer. It is high during a Read operation and low during a Write operation.
33–40, M, N, P, R–V	A0–A15	Address Bus—The address-bus lines are outputs from the processor that carry the desired address to the peripherals.
F	VMA	Valid Memory Address—The valid memory address line is a processor output that is high when the address-bus lines contain a valid address (normally during the clock $\phi 1$).

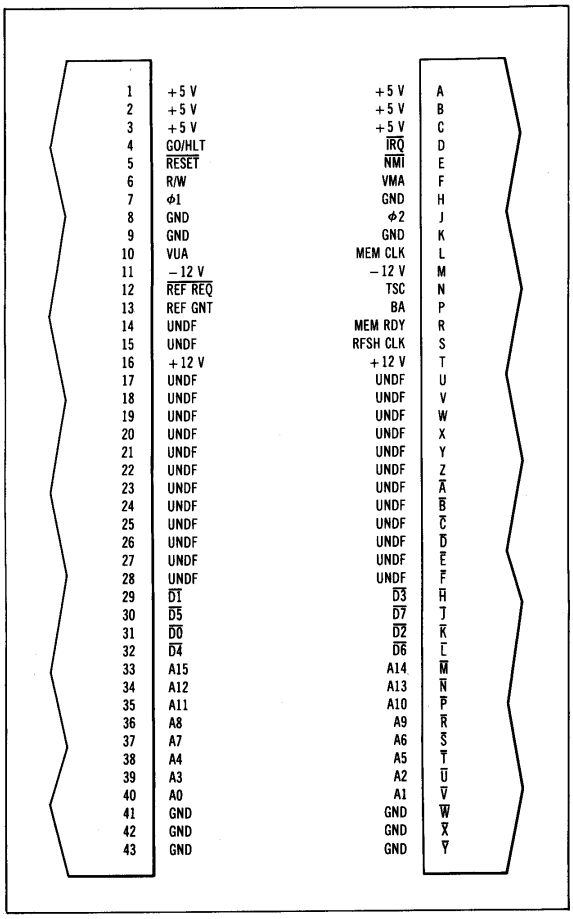
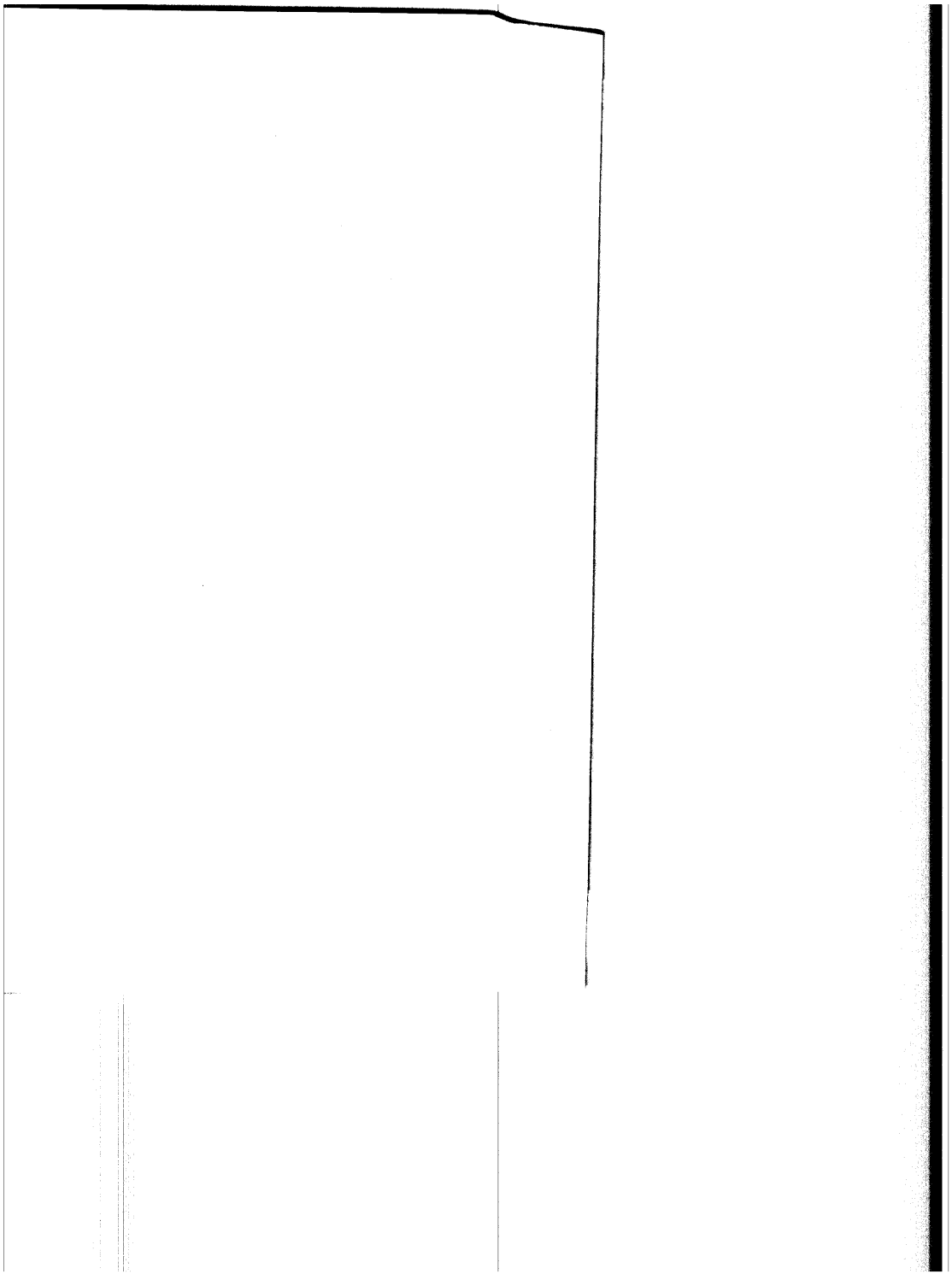


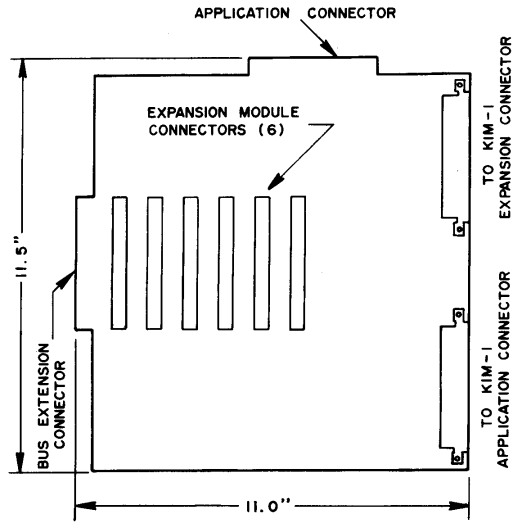
Fig. 8-3. The Exorcisor bus pinout designations.

Pin No.	Signal	Definition
		In an Exorcisor system, the VMA feeds only the executive DEBUG module, which generates the VUA signal.
10	VUA	Valid User Address—The valid user address line is a DEBUG module output that is high when the address bus contains a valid address for any location other than one in the EXBUG monitor. It replaces the VMA for peripherals.
5	$\overline{\text{RESET}}$	Reset—The reset line is the output of a one-shot used to reset the processor and peripherals. An input cannot be applied to this line without circuit modification.
E	$\overline{\text{NMI}}$	Nonmaskable Interrupt—The nonmaskable interrupt input feeds the processor's NMI. When pulled low by a peripheral, the processor finishes the current instruction, stores the internal registers on the stack, loads the NMI vector into the program counter and begins execution of the NMI service routine.
D	$\overline{\text{IRQ}}$	Interrupt Request—The interrupt request input feeds the IRQ of the processor. When pulled low by a peripheral, the processor finishes the current instruction, checks the "I" flag in the CCR and, if it is reset, stores the internal registers on the stack. It, then, loads the IRQ vector into the program counter and begins execution of the IRQ service routine.
4	GO/HLT	Go/Halt—The go/halt line is an input to the halt line of the processor. When pulled low, it causes the processor to suspend all operations, pull the BA high, pull the VMA low and put all other lines in a high-impedance state.
P	BA	Bus Available—The bus-available line is an output that indicates whether the processor is running or has been stopped. It is low when the processor is executing a program. It is pulled high when the processor is stopped by the Halt input or the execution of a wait instruction. By watching the BA line, an external device can verify that the processor has stopped and its lines are floating, thus, allowing DMA.
N	TSC	Three-State Control—The three-state control line is an input to the processor that, when pulled high, causes the address bus and R/W line to float and pulls the VMA and BA low. An external device can then use the address bus in DMA operations. The system clock must also be stopped with $\phi 1$ high and $\phi 2$ low. Unfortunately, the clock can be stopped for only a short period of time since the processor is a dynamic chip.
7, J	$\phi 1$, $\phi 2$	$\phi 1$, $\phi 2$—The two phase, nonoverlapping system clock which synchronizes all operations.
R	MEM RDY	Memory Ready—The memory-ready line is an input to the system clock circuitry that allows the processor to work with slow memories by stretching the $\phi 2$ signal. (Stretching a clock cycle is momentarily stopping the clock while both $\phi 1$

Pin No.	Signal	Definition
		and $\phi 2$ signals are held steady.) When pulled low by address decoding logic associated with slow memory, the $\phi 2$ clock signal is lengthened. This gives the memory more time to present data to or take data from the data bus. The $\phi 2$ signal is stretched since all data transfers occur during its occurrence.
L	MEM CLK	Memory Clock—The memory clock line is a $\phi 2$ output of the system clock circuitry. It leads the $\phi 2$ signal by about 10 ns. It is used by dynamic memory circuits to synchronize refresh operations with the processor. It is not affected by clock stretching signals.
S	$\overline{\text{REF CLK}}$	Refresh Clock—The refresh clock is the output of an astable multivibrator in the dynamic memory refresh circuitry. It is used to generate the $\overline{\text{REF REQ}}$ signal and to control the refresh counters.
12	$\overline{\text{REF REQ}}$	Refresh Request—The refresh request line is an input to the system clock that is driven by the refresh circuitry on a dynamic memory board. The $\overline{\text{REF REQ}}$ is pulled low periodically to inform the processor of the need to refresh dynamic RAM. The processor responds to this signal with the REF GNT, which sets the $\overline{\text{REF REQ}}$ high, clearing it.
13	REF GNT	Refresh Grant—The refresh grant line is an output of the system clock generator that acknowledges an input on the $\overline{\text{REF REQ}}$ line. When the $\overline{\text{REF REQ}}$ is received, the REF GNT is pulled high at the beginning of the next clock $\phi 1$. This signal clears the $\overline{\text{REF REQ}}$ and indicates that the cycle beginning can be used as a refresh cycle. The $\phi 1$ signal is stretched during the refresh and the processor continues program execution during the following $\phi 2$ cycle. Refreshing dynamic RAM in this manner is known as cycle stealing.
1, 2, 3, A, B, C	+5 V	+5 V—The +5 V dc line is a regulated power input that should be able to supply 15 amperes.
16, T	+12 V	+12 V—The +12 V dc line is a regulated power input that should be able to supply 2.5 amperes.
11, M	−12 V	−12 V—The −12 V dc line is a regulated power input that should be able to supply 1.0 ampere.
8, 9, 41-43, H, K, $\overline{\text{W}}$-$\overline{\text{Y}}$	GND	Ground—The ground line is the common return for all system supplies and signals.
14, 15, 17–28, U–Z, $\overline{\text{A}}$–$\overline{\text{F}}$	UNDF	Undefined—These lines are undefined on the bus and may be dedicated to special functions by the user.



expansion motherboard that plugs directly onto the KIM-1, the KIM-4 buffers all signals and provides connection slots for six additional boards, each of which uses KIM-4 bus. The KIM-4 includes address decode circuitry that activates the KIM-1 memory (when called). The pinout designations for the KIM-4 board are shown in Fig. 9-6.



Courtesy MOS Technology, Inc.

Fig. 9-5. Diagram of the KIM-4 motherboard.

Pin No.	Signal	Definitions
8–15	BDB0–BDB7	Data Lines—This is the buffered bidirectional data bus line.
W	BR/W	Read/Write—This is the buffered read/write line.
2	BSYNC	BSYNC—This is the buffered sync line.
3	$\overline{\text{BRDY}}$	Ready—This is the buffered ready line.
B–F, H, J–N, P, R–T, U	BAB0–BAB15	Address Bus—This is the buffered address bus.

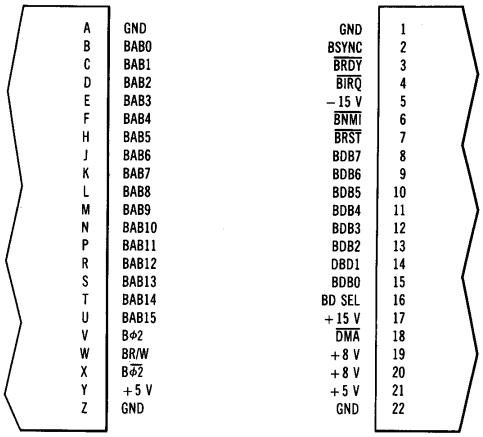


Fig. 9-6. Bus pinout designations for the KIM-4 board.

Pin No.	Signal	Definitions
7	$\overline{\text{BRST}}$	Reset—This is the buffered reset line.
6	$\overline{\text{BNMI}}$	Nonmaskable Interrupt—This is the buffered nonmaskable interrupt line.
4	$\overline{\text{BIRQ}}$	Interrupt Request—This is the buffered interrupt request line.
V	Bϕ2	ϕ2—The buffered ϕ2 clock line.
X	B$\overline{\phi 2}$	ϕ2—The buffered ϕ2 clock line inverted.
18	$\overline{\text{DMA}}$	Direct Memory Access—The direct memory access line is an input which, when pulled low, causes the data and address buses and the read/write line to float. Floating these lines means their buffers enter a high impedance state which effectively disconnects the expansion bus from the processor. An external device such as a disk controller can then use the bus to load from or dump to the memory.
21, Y	+5 V	+5 V—The +5 V dc line provides a regulated +5 V dc for the KIM-1.
19, 20	+8 V	+8 V—The +8 V dc line provides unregulated power to each of the expansion boards which must contain regulation circuitry. The +8-volt supply should be capable of producing 15 amperes.
17	+15 V	+15 V—The +15 V line is an input that feeds a +12-volt regulator. The regulated +12 volts is passed to the KIM-1 for use in the audio interface circuitry.
5	−15 V	−15 V—The −15 V line is an unregulated input that is

Pin No.	Signal	Definitions
		passed to each of the expansion boards where (if needed) it can be regulated.
1, 22, A, Z	GND	Ground—The ground line is the common return line for all system power supplies and signal lines.
16	BD SEL	This is an unused line common to all KIM-4 boards.

KIM-1 APPLICATION-CONNECTOR SIGNAL DEFINITIONS

Expansion of the KIM-1 is also possible through its application connector which provides I/O lines. The KIM-1 application connector is duplicated pin for pin on the KIM-4 motherboard except as noted in the signal definitions. The application-connector pinout designations for the KIM-1 are shown in Fig. 9-7.

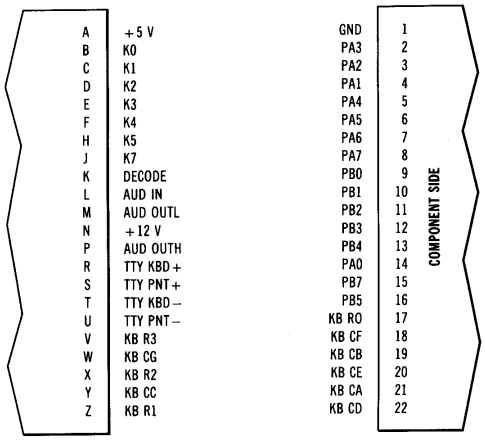


Fig. 9-7. Application pinout designations for the KIM-1.

Pin No.	Signal	Definition
2–8, 14	PA0–PA7	I/O Lines—PA0–PA7 are the user accessible I/O lines of Port A, a bidirectional programmable parallel port that rests at Hex locations 1700 and 1701 on the 6530-003 integrated circuit. Each line may be individually programmed as an input or output; each is capable of driving one standard TTL load.

Pin No.	Signal	Definition
9–13, 15, 16	PB0–PB5, PB7	I/O Lines—PB0–PB5 and PB7 are the user accessible I/O lines of Port B, a bidirectional programmable parallel port that rests at Hex locations 1702 and 1703 on the 6530-003 integrated circuit. Each line is TTL compatible. Only seven lines are available for I/O since the line normally used for PB6 has been dedicated as a chip select.
18–22, W, Y	KB CA–KB CG	Keyboard Column—These lines are I/O lines PA0–PA6 of Port A on the 6530-002 integrated circuit. The KIM-1 uses these lines in the strobed Hex keyboard and display. They are available to allow a remote keyboard. They can, however, also be used to I/O lines during program execution.
17, V, X, Z	KB R0–KB R3	Keyboard Row—These lines are the output of a decimal decoder used by the KIM-1 (in conjunction with the keyboard column lines) to scan the Hex keyboard. They are provided to allow a remote keyboard.
L	AUD IN	Audio Input—The audio input line that is used to connect the earphone jack of an audio tape recorder to the on-board audio interface.
M, P	AUD OUT (Hi and Lo)	Audio Output—The audio output lines connect the on-board audio interface to the microphone input on an audio tape recorder. The low output is normally used although recorders that have an auxiliary input may operate with the high output.
R, T	TTY KY (+ and —)	Teletype Keyboard—These lines provide a 20-mA current loop that can be driven by a teleprinter keyboard.
S, U	TTY PTR (+ and —)	Teletype Printer—These lines provide a 20-mA current loop that can drive a teleprinter print mechanism.
B–F, H, J	K0–K7	K0–K7—These lines are the outputs of a decimal decoder. They serve as chip select lines for the first eight kilobytes of memory. See Fig. 9-2 for memory-map details.
K	DECODE	Decode—The decode line is an input to the K0–K7 decoder. It must be held low to enable the decoder and to use memory on the KIM-1. Expansion beyond eight kilobytes requires that the external logic control the decode line to choose on- or off-board memory.
A	V_{CC}	V_{CC}—This is a +5 V dc regulated input.
1	GND	Ground—The ground line is the V_{CC} return.
N	+12 V	+12 V—The +12-volt line.

DISCUSSION

KIM-1 expansion is often performed with S-100 boards since the KIM-compatible boards are scarce and expensive while the S-100 boards are plentiful and inexpensive. A commercially available interface board is discussed in Chapter 15.

CHAPTER 10

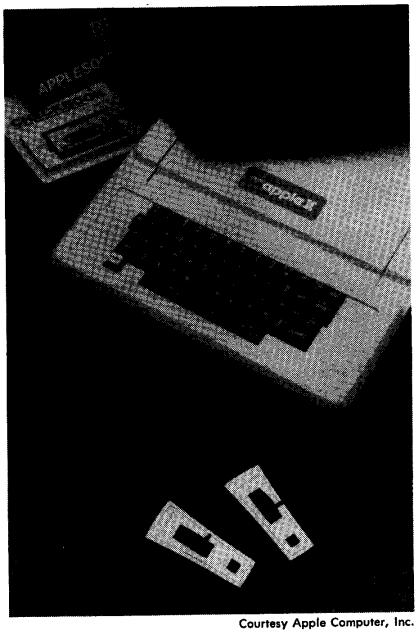
The Apple II Bus

The Apple II microcomputer, shown in Fig. 10-1, is a single-board system that includes a processor, operating system, and BASIC in ROM, RAM, keyboard, color video-display generator, cassette interface, power supply, speaker, and game paddles. In addition to the speaker and game paddles, the Apple II comes equipped with demonstration tapes, instruction manual, and your choice of either 8K or 16K of memory. Packaged in a compact plastic case, it has been a popular system.

Memory expansion is extremely simple on the Apple microcomputer. Three rows of sockets are provided that will support either 4- or 16-kilobit dynamic RAMs. The system can be expanded by simply filling the existing sockets with chips or by replacing 4-kilobit chips with 16-kilobit chips. A maximum of 48 kilobytes of RAM is possible using these sockets.

A motherboard area (containing 8 sockets) is also provided. It is located at the back of the main circuit board as shown in Fig. 10-2. All signals necessary to add memory or peripherals are available at these connectors.

A variety of expansion boards, like the one shown in Fig. 10-3, are offered by Apple Computer, Inc. The expansion boards are 2¾ inches × 7 inches in size and use a double-sided, 50-pin (25 each side), edge-card connector with 0.1-inch spacing. The connectors are offset as shown in Fig. 10-3, providing positive indexing for the boards. The expansion board shown in Fig. 10-3 is Apple's Model A2B0003X Communications Card. It permits the Apple II to serve as a terminal in a time-sharing network or within a network of two or more Apple computers that have access to and control of other Apple II computers.



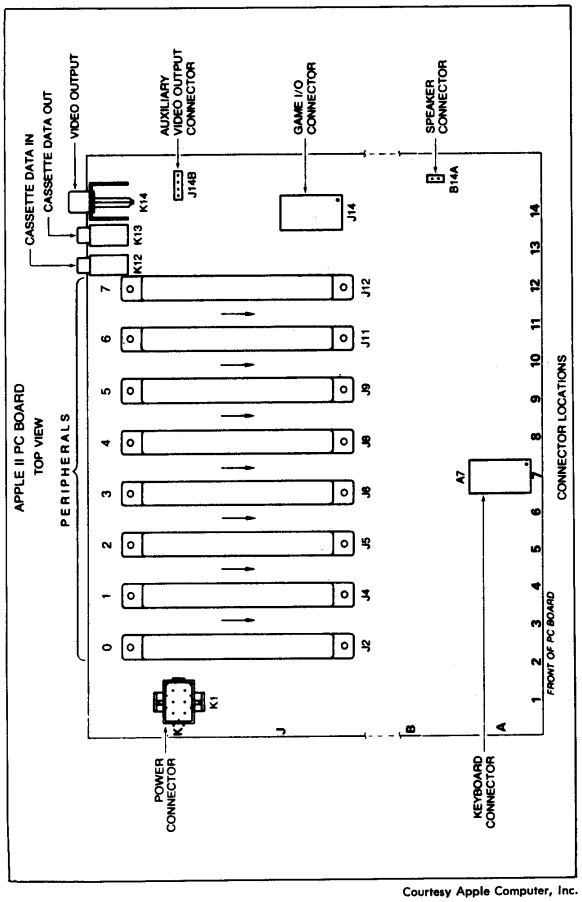
Courtesy Apple Computer, Inc.

Fig. 10-1. The Apple II microcomputer.

APPLE II SIGNAL DEFINITIONS

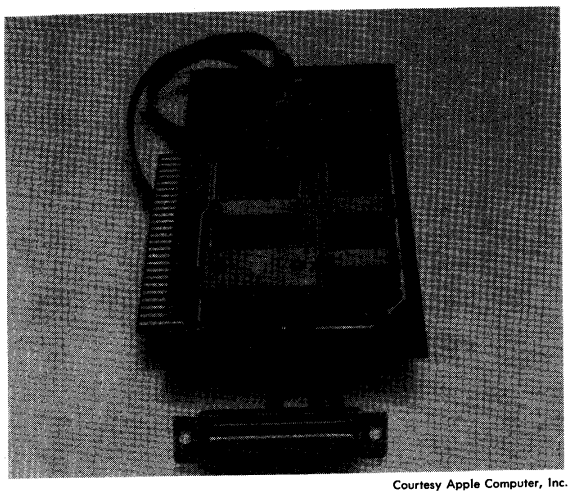
The Apple II bus pinout designations are shown in Fig. 10-4.

Pin No.	Signal	Definition
42–49	D0–D7	Data Lines—These are bidirectional, buffered data lines of the processor. They carry information into and out of the processor.
18	R/$\overline{W}$	Read/Write—The buffered read/write line of the processor is used to control the direction of data flow on the data lines. When high, a Read operation will occur, when low, a Write operation will occur.
21	$\overline{RDY}$	Ready—The ready line is a processor input that, when pulled low during $\phi 1$, will halt the processor during



Courtesy Apple Computer, Inc.

Fig. 10-2. The Apple II pc board showing the "motherboard area" located at the rear of the main board.



Courtesy Apple Computer, Inc.

Fig. 10-3. A serial-communications expansion board.

Pin No.	Signal	Definition
		the next $\phi 1$ cycle. When it is pulled high, execution will continue in the following $\phi 2$. Slow memory can use the ready line to gain the extra time needed to access data. The Ready will not halt the processor during a Write operation, but in the $\phi 1$ that follows.
2–17	A0–A15	Address Lines—The buffered address lines of the processor carry the location of the desired data from the processor to the peripherals.
20	$\overline{\text{I/O STROBE}}$	I/O Strobe—The I/O strobe is an active low output. It is pulled low on all connectors when a Hex address between C800 and CFFF is called by the processor. It can be used as a chip select signal. (See the memory map of Fig. 10-5.)
41	$\overline{\text{DEVICE SELECT}}$	Device Select—The device select line is an active low output that is pulled low on only one connector at a time in response to predetermined addresses. As shown in Fig. 10-5, each connector is assigned 16 unique addresses that are associated with the device select. When an address assigned to a connector is called, the device select line is pulled low on only that connector. This line can be used as a chip select signal.

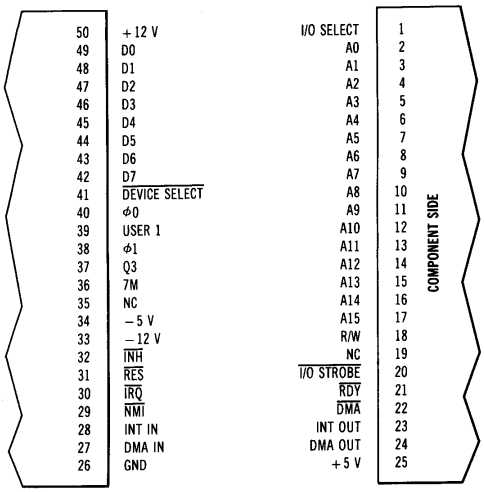


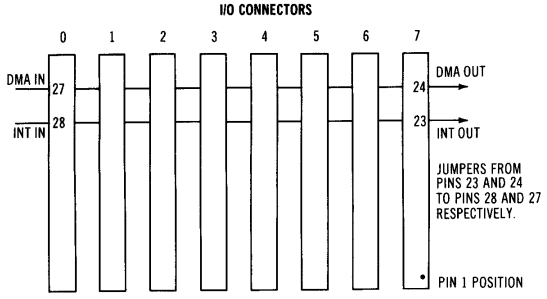
Fig. 10-4. The Apple II bus pinout designations.

Pin No.	Signal	Definition
1	I/O SELECT	I/O Select—The I/O select is an active low output that, like the device select, is pulled low on only one connector at a time, in response to a specific group of addresses. As shown in Fig. 10-5, each connector, except No. 0, is assigned 256 unique addresses that are associated with the I/O select. When an address assigned to a connector is called, the I/O select line is pulled low on only that connector. This line can be used as a chip select signal.
32	INH	Inhibit—The inhibit line is an input that, when pulled low, disables all on-board ROMs, thus allowing the use of customized operating system software.
31	RES	Reset—The reset line is an input to the active low reset of the processor. Pulling this line low will cause the processor to cease its current operation and return to the system monitor.
29	NMI	Nonmaskable Interrupt—The NMI line is an input to the active low NMI of the processor. When pulled low, the processor will finish the current instruction, push the program counter and status register onto the stack, load the contents of the NMI vector into the program

HEX ADDRESS	PIN FUNCTION
CFFF C800	THE I/O STROBE IS PULLED LOW ON ALL CONNECTORS.
C7FF C700	THE I/O SELECT IS PULLED LOW ON CONNECTOR 7.
C6FF C600	THE I/O SELECT IS PULLED LOW ON CONNECTOR 6.
C5FF C500	THE I/O SELECT IS PULLED LOW ON CONNECTOR 5.
C4FF C400	THE I/O SELECT IS PULLED LOW ON CONNECTOR 4.
C3FF C300	THE I/O SELECT IS PULLED LOW ON CONNECTOR 3.
C2FF C200	THE I/O SELECT IS PULLED LOW ON CONNECTOR 2.
C1FF C100	THE I/O SELECT IS PULLED LOW ON CONNECTOR 1.
C0FF C0F0	THE DEVICE SELECT IS PULLED LOW ON CONNECTOR 7.
C0EF C0E0	THE DEVICE SELECT IS PULLED LOW ON CONNECTOR 6.
C0DF C0D0	THE DEVICE SELECT IS PULLED LOW ON CONNECTOR 5.
C0CF C0C0	THE DEVICE SELECT IS PULLED LOW ON CONNECTOR 4.
C0BF C0B0	THE DEVICE SELECT IS PULLED LOW ON CONNECTOR 3.
C0AF C0A0	THE DEVICE SELECT IS PULLED LOW ON CONNECTOR 2.
C09F C090	THE DEVICE SELECT IS PULLED LOW ON CONNECTOR 1.
C08F C080	THE DEVICE SELECT IS PULLED LOW ON CONNECTOR 0.

Courtesy Apple Computer, Inc.

Fig. 10-5. Special I/O connector select addresses.



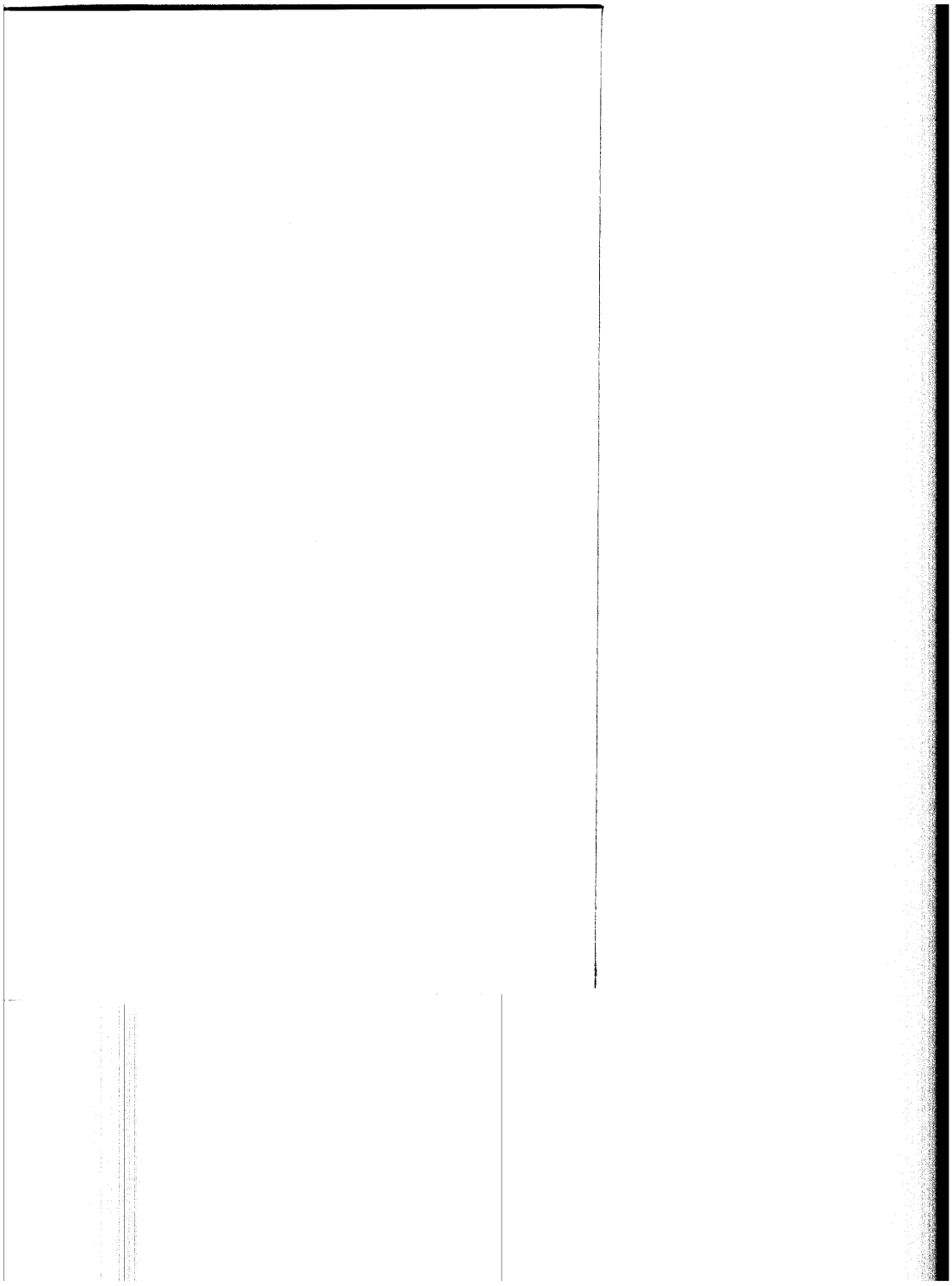
Courtesy Apple Computer, Inc.

Fig. 10-6. The INT IN/INT OUT and DMA IN/DMA OUT "daisy chains" on the I/O connectors.

Pin No.	Signal	Definition
		counter and, then, begin executing the NMI service routine.
30	$\overline{IRQ}$	Interrupt Request—The IRQ line is an input to the active low IRQ of the processor. When pulled low, the processor will finish the current instruction and check the "I" status flag. If it is reset, the program counter and status register will be pushed onto the stack, the contents of the IRQ vector will be loaded into the program counter and execution of the IRQ service routine will begin. If the "I" flag is set, the processor will ignore an IRQ input until it is reset.
23, 28	INT IN, INT OUT	Interrupt Input and Interrupt Output—The INT IN and INT OUT lines allow the implementation of a simple interrupt priority scheme in a system that has more than one source of interrupts. The INT OUT line of each connector runs to the INT IN of the next connector to form the simple "daisy chain" shown in Fig. 10-6. The status of these lines determines when a board can request service on the NMI or IRQ lines. When an interrupt is generated on a board, the board cannot signal the IRQ until it checks the status of its INT IN. If the INT IN of the board is low, a higher priority board is using the IRQ and the board must wait until the INT IN is returned high. If the INT IN is high, or is returned high, the board can use the IRQ but it must first pull its INT OUT low, thereby indicating a busy IRQ to boards with lower priority. Each board must pass a busy signal on to lower priority boards by pulling its INT OUT low when the

Pin No.	Signal	Definition
		INT IN of the board is pulled low. Using this scheme, the board in connector 0 has the highest priority and the board in position 7 has the lowest. Any board not using interrupts must pass the INT IN to the INT OUT with a jumper to prevent a break in the chain. All hardware needed to implement this system must be contained on the peripheral boards. It is important to note that use of the INT IN and INT OUT is completely optional. The NMI and IRQ are provided at each connector and can be used as desired with or without the use of the INT IN and INT OUT.
40	$\phi 0$	Clock Phase Zero—This signal is derived from the master oscillator and is used to drive the clock input of the processor. Using this signal, the processor produces the $\phi 1$ and $\phi 2$ signals for the system. This $\phi 0$ signal can be used the same as $\phi 2$ since they are functionally the same.
38	$\phi 1$	Clock Phase One—The $\phi 1$ signal is one output of the system clock generator of the processor.
36	7M	7-MHz Clock—This 7-MHz signal is derived from the master oscillator and is available for use by peripherals.
37	Q3	Q3—The Q3 is a 2-MHz signal derived from the master oscillator. It is available for use by peripherals.
22	$\overline{\text{DMA}}$	Direct Memory Access—The $\overline{\text{DMA}}$ line can be used by peripherals to gain control of the buses of the system. Pulling this line low floats the address and read/write lines and inhibits the $\phi 0$ clock input, effectively stopping the processor and putting the data lines in the input mode. A peripheral can then use the buses for DMA operations. Since the 6502 is a dynamic device, the clock can only be stopped for a maximum of 1 ms before the internal register contents are lost. Therefore, the DMA must be completed in less than 1 ms.
24, 27	DMA IN, DMA OUT	Direct Memory Access In and Direct Memory Access Out—The DMA IN and DMA OUT lines allow the implementation of a DMA priority scheme much like the interrupt priority that was obtained using the INT IN and INT OUT lines. The DMA IN and DMA OUT lines are connected (Fig. 10-6) to form a "daisy chain" which functions like the INT IN and INT OUT chain. Use of the DMA IN and DMA OUT lines is completely optional, the $\overline{\text{DMA}}$ functions without their use.
39	USER 1	User 1—The User line is an input to the address decoder that generates the I/O and ROM enable signals. Pulling this line low disables the I/O enable signals and all on-board ROM, thus allowing different

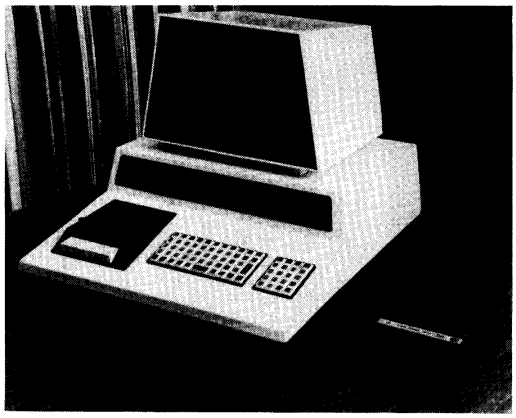
Pin No.	Signal	Definition
		implementation of the memory space between Hex C000 and FFFF.
19, 35	NC	No Connection—The NC contact is undefined and available for use.
25	+5 V	+5 V—The +5 V dc line is a regulated output that can provide up to 500 mA.
50	+12 V	+12 V—The +12 V dc line is a regulated output that can provide up to 250 mA.
34	−5 V	−5 V—The −5 V dc line is a regulated output that can provide up to 200 mA.
33	−12 V	−12 V—The −12 V dc line is a regulated output that can supply up to 200 mA.
26	GND	Ground—The ground line is the common return for the signal and power lines of the system.



CHAPTER 11

The PET Bus

Commodore Business Machines' PET, shown in Fig. 11-1, is one of the new breed of microcomputers. They are complete systems in a single package. The PET system provides CPU, RAM, system executive and BASIC in ROM, integral alphanumeric keyboard and CRT display, cassette recorder and interface, programmable I/O



Courtesy Commodore Business Machines, Inc.

Fig. 11-1. The PET system.

lines, and instrumentation provisions in an attractive case. The user has only to plug the unit in and turn it on to get started in a BASIC operating system. Introduced in 1977, the PET has been very popular. Several expansion modules for the system are currently being offered.

Expansion of the 6502-based system is relatively easy. All of the expansion lines are buffered and the expansion memory is decoded into 4-kilobyte blocks. Expansion of the PET is performed via a 40-pin edge-card connector (with 0.100-inch spacing) that protrudes from the right side of the PET. All of the pins on the top side of the connector are grounded. No positive indexing is provided.

PET EXPANSION-CONNECTOR SIGNAL DEFINITIONS

The PET expansion-connector pinout designations are shown in Fig. 11-2.

Pin No.	Signal	Definition
1–79	—	All odd numbered pins are grounded.
66, 68, 70, 72, 74, 76, 78, 80	D0–D7	Data Bus—The bidirectional data bus lines carry data between the processor and the peripherals.
60	R/W	Read/Write—The read/write line is an output used by the processor to control direction of data movement on the data bus. When high, the processor is reading data; when low, it is writing data.
2, 4, 6, 8, 10, 12, 14, 16, 18, 20, 22, 24	A0–A11	Address Bus—The address bus lines are outputs that are used by the processor, in conjunction with the select lines, to specify the location desired.
32, 34, 36, 38, 40, 42, 44, 46, 48, 50	SEL1–SEL7, SEL9–SELB	Select—The select lines are the decoded address outputs of the A12–A15 lines of the processor, that do not appear on the connector. SEL1–SELB are used to select, or enable, 4-kilobyte blocks of expansion memory or I/O. Select line 1 enables the 4-kilobyte block between Hex 1000 and 1FFF, Select line 2 enables addresses between Hex 2000 and 2FFF, etc. The processor uses the select signals to indicate a specific 4-kilobyte block and the A0–A11 lines to indicate the desired byte in that block. The memory map for the PET is shown in Fig. 11-3. Dedicated and user-available areas are defined using the SELECT lines.
54	$\overline{\text{RES}}$	Reset—The reset line is an unbuffered input to the reset line of the processor. Pulling this line low causes the proces-

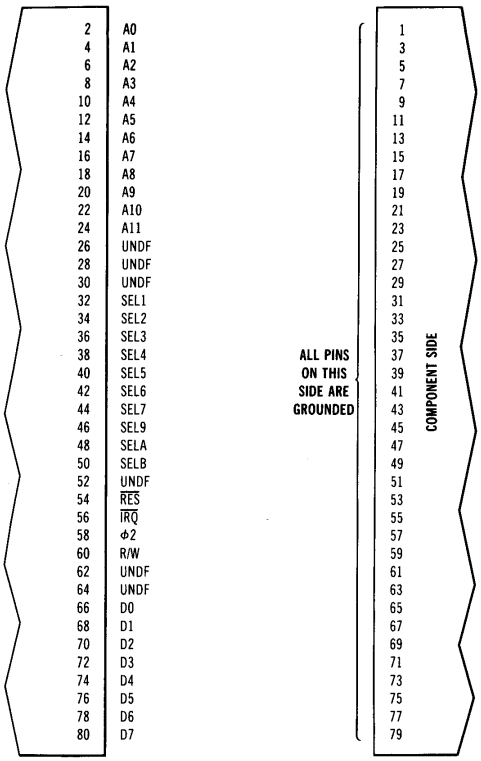
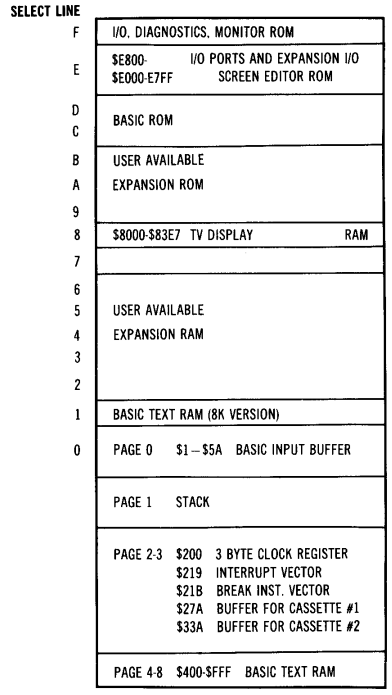


Fig. 11-2. The PET expansion-connector pinout designations.

Pin No.	Signal	Definition
		sor to load the program counter with the contents of the reset vector and to begin execution.
56	$\overline{IRQ}$	Interrupt Request—The interrupt request line is an unbuffered input to the IRQ of the processor. When pulled low, the processor examines the "I" flag and, if reset, sets the "I" flag, stores the PC and status register on the stack, loads the PC with the contents of the IRQ vector and be-

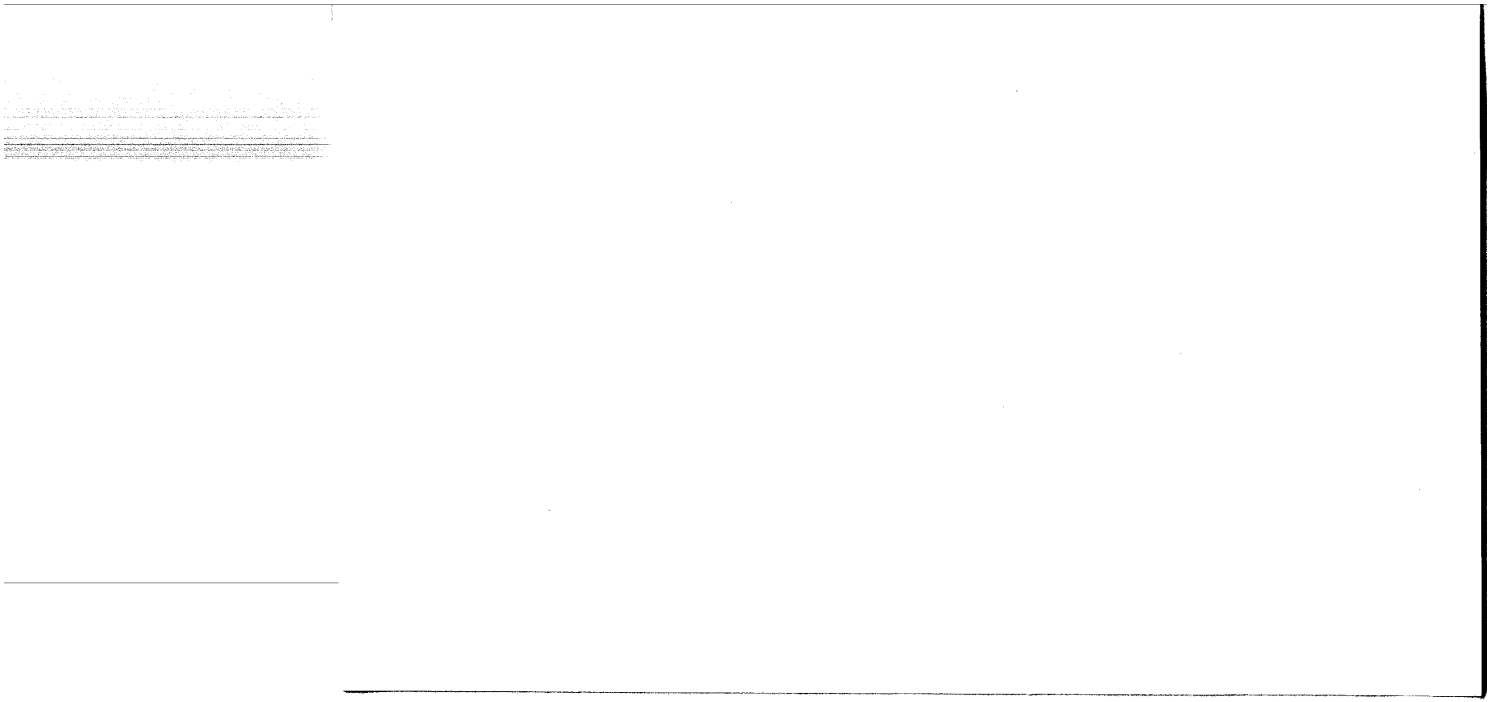


Courtesy Commodore Business Machines, Inc.

Fig. 11-3. The PET memory map.

Pin No.	Signal	Definition
		gins execution of the IRQ service routine. If the "I" flag is set when the IRQ is pulled low, the processor will ignore the IRQ until the "I" is reset.
58	$\phi 2$	$\phi 2$—The $\phi 2$ line is the output of the system clock and can be used as a chip enable since all data movement occurs during $\phi 2$.
26, 28, 30, 52, 62, 64	UNDF	Undefined—These lines are not assigned a function by the PET and can be used externally for user desired functions.

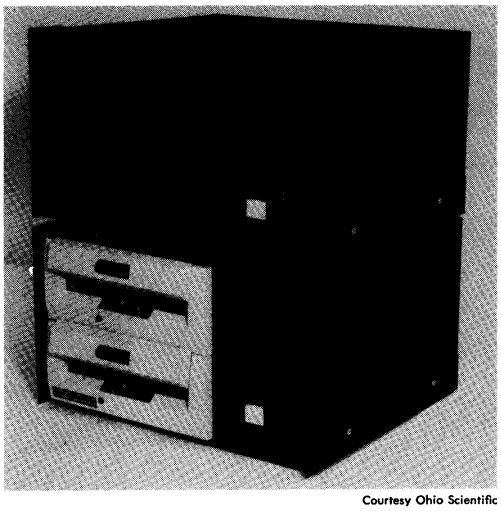
Several companies are producing PET-to-S-100 interface boards that allow PET owners to use the many available S-100 boards. See Chapter 15 for further details.



CHAPTER 12

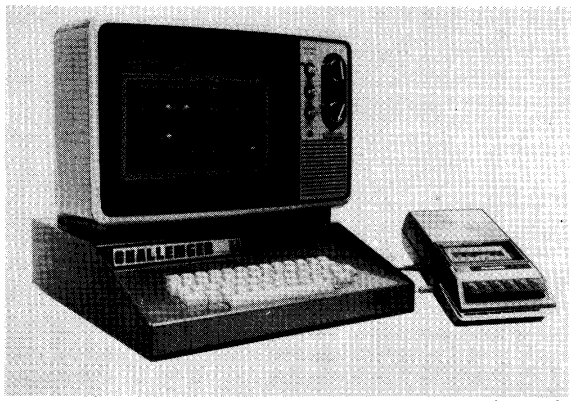
The Ohio Scientific Bus

The standard 48-line system bus developed in 1975 by Ohio Scientific is used today throughout their broad line of products. Over 40 bus-compatible boards are presently available from Ohio Scientific. They also offer a variety of bus-compatible microcomputers



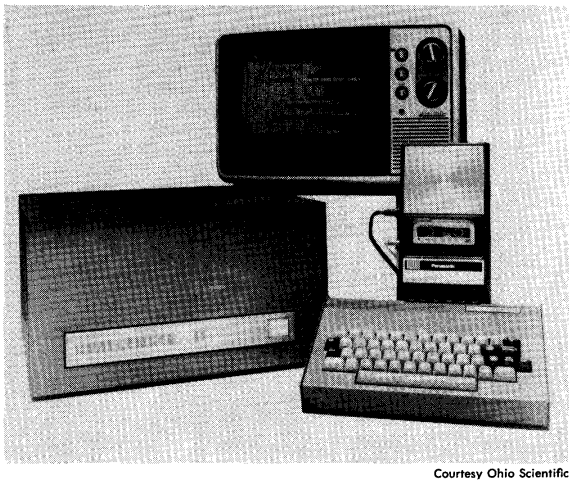
Courtesy Ohio Scientific

Fig. 12-1. The Challenger III microcomputer.



Courtesy Ohio Scientific

Fig. 12-2. The Challenger C2-4P microcomputer.



Courtesy Ohio Scientific

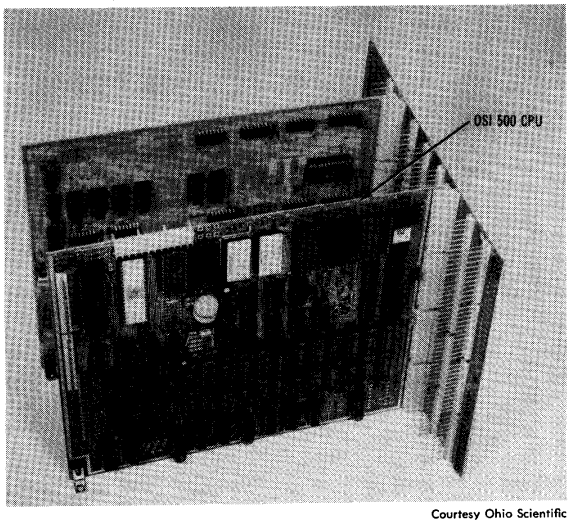
Fig. 12-3. The Challenger C2-8P microcomputer.

that range from the expandable business system shown in Fig. 12-1 to the simple turn-key system illustrated in Fig. 12-2. The C2-4P (Fig. 12-2) and the C2-8P (Fig. 12-3) are part of Ohio Scientific's Challenger IIP series. These are ultra high-performance bus-oriented microcomputers for personal, educational, research, and small business use. Both microcomputers are also available in color versions.

Ohio Scientific systems are primarily 6502 based although, a multiprocessor board featuring 6502, 6800, and Z80 micros is available. Ohio Scientific boards are 8 inches × 10 inches in size and plug into the backplane connector shown in Fig. 12-4. All the boards use four 12-pin KK-156 Molex connectors to mate with the 48-pin bus. No positive indexing is provided.

BUS SIGNAL DEFINITIONS

The pinout designations of the Ohio Scientific bus are shown in Fig. 12-5.



Courtesy Ohio Scientific

Fig. 12-4. The OS-48 motherboard.

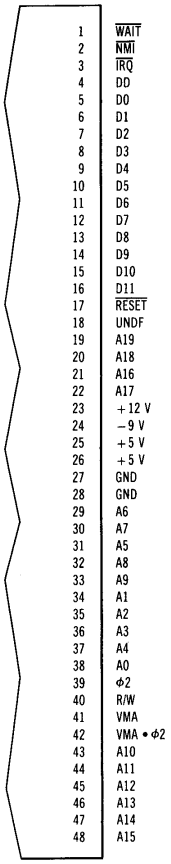


Fig. 12-5. The OS-48 pinout designations.

Pin No.	Signal	Definition
5–12	D0–D7	Data Line—The bidirectional data bus which carries information between the processor and all the peripherals.
40	R/W	Read/Write—This line is a processor output that directs data flow on the data bus. When high, a Read operation will occur; when low, a Write operation will occur.
4	DD	Data Direction—The data direction line is an input to the processor board that is used by peripherals to control its data bus buffers. When a peripheral board, after responding to the address bus (R/W) and $\phi 2$ lines, has valid data for or can accept valid data from the processor, it pulls the data direction line high for a Write operation or, low for a Read operation.
39	$\phi 2$	Clock Phase Two—The clock $\phi 2$ output of the processor. All data transfers take place during the $\phi 2$ period.
41	VMA	Valid Memory Address—The valid memory address is the output of the VMA line of the 6800 microprocessor. The processor pulls the VMA high during clock $\phi 1$, after the desired address is placed on the address bus and is settled. The 6502 processor does not have a VMA line so, in 6502 systems, line number 41 is permanently pulled high.
42	VMA $\phi 2$	VMA $\phi 2$—This line is the output of an AND gate that is fed to peripheral boards to serve as a chip enable line. When high, a data transfer can occur with little possibility of error caused by unsettled lines. Since the 6502 has no VMA line, the VMA $\phi 2$ line on 6502 systems is the $\phi 2$ line of the processor.
29–38, 43–48	A0–A15	Address Bus—The address bus lines are processor outputs which carry the desired address to the peripherals.
19–22	A16–A19	Upper Address—These upper address lines are used to provide additional addressing capability in systems that are expanded with floppy disks. Signals A16–A19 are not inherent to either the 6502 or the 6800. They are derived by using four 6820 peripheral interface adapter lines configured as outputs. They are software controlled.
2	$\overline{\text{NMI}}$	Nonmaskable Interrupt—This is the unbuffered nonmaskable interrupt input to the processor. When pulled low, the processor finishes execution of the current instruction, pushes some internal registers onto the stack, loads the contents of the NMI vector into the program counter and begins execution of the interrupt service routine. The ACCA, ACCB, INX, PC and condition-code registers are all automatically saved on the stack in the 6800, while the 6502 saves only the PC and condition-code registers. The processor must respond to a NMI request for service.
3	$\overline{\text{IRQ}}$	Interrupt Request—The interrupt request input is the unbuffered input to the IRQ line of the processor. When pulled low, the processor will finish execution of the current instruction and push some internal registers (see NMI) onto

Pin No.	Signal	Definition
		the stack. It then sets the "I" flag, loads the program counter with the contents of the IRQ vector and begins execution of the service routine. The processor will respond to an IRQ request only if the "I" flag in the status is reset when the request occurs.
1	$\overline{\text{WAIT}}$	Wait—The wait line is an input that allows external control of the clock frequency of the processor. The line is used to switch diodes which add resistance to the RC circuit of the astable multivibrator clock, thereby changing the frequency. Pulling the WAIT line low slows the clock to about 500 kHz to allow easy interface with slow memory and peripherals. The WAIT line will not be active in systems which are configured for a single clock speed.
17	$\overline{\text{RESET}}$	Reset—The reset line is an optional line that may, in some systems, be used to reset peripheral interface adapters.
13–16	D8–D11	Upper Data—Optional data bus lines that may be used if a 12-bit processor (the Intersil 6100) is added to the system. They are not inherent to either the 6502 or the 6800 or their systems.
18	UNDF	Undefined—The undefined line has no dedicated use and may be used to perform special or custom functions.
25, 26	+5 V	+5 V—This line is a power input that requires +5 V dc at 2.0 amperes regulated voltage.
23	+12 V	+12 V—This line is a power input that requires +12 V dc at 0.5 ampere regulated voltage.
24	−9 V	−9 V—This line is a power input that requires −9 V dc at 0.5 ampere regulated voltage.
27, 28	GND	Ground—The ground line is the common return for all system power supplies and signal lines.

All lines except the $\overline{\text{NMI}}$, $\overline{\text{IRQ}}$, and $\overline{\text{RES}}$ lines are buffered. It should be noted that the processor Reset line is not on the system bus. It is, instead, available on an auxiliary connector that is located on the CPU board.

AUXILIARY-CONNECTOR SIGNAL DEFINITIONS

Many of the systems offered by Ohio Scientific are based on their Model 500 CPU board, which is the nearest board shown in Fig. 12-4. Since it is so widely used, its auxiliary connector (AX) will be defined. The auxiliary connector accepts a KK-156 Molex connector which is located in the upper left-hand corner of the Model 500 board (Fig. 12-4). The pinout designations of the auxiliary connector are shown in Fig. 12-6.

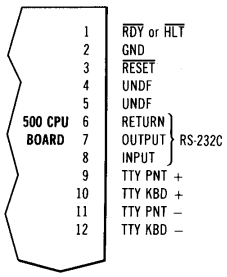
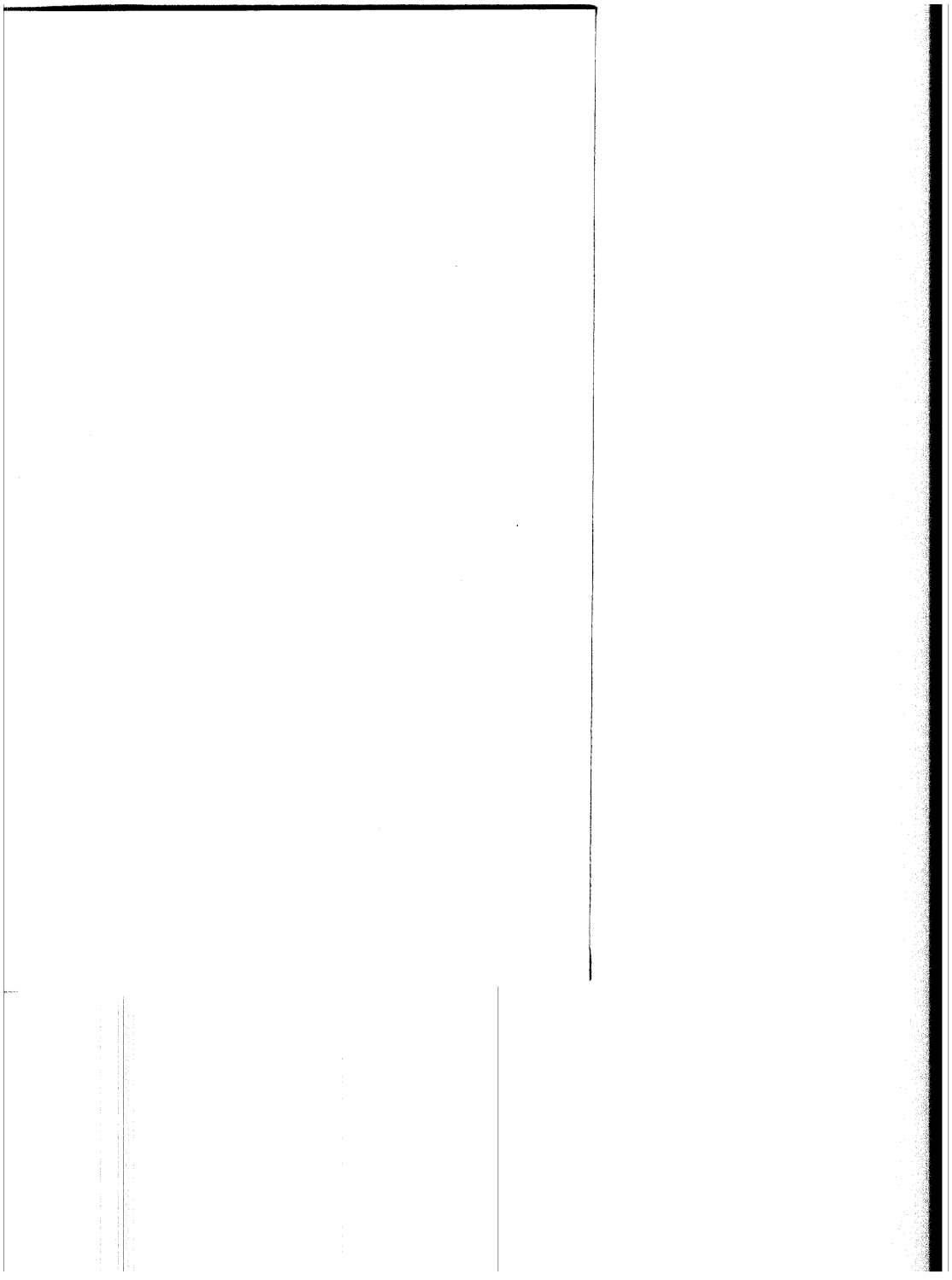


Fig. 12-6. Pinout designations for the auxiliary connector.

Pin No.	Signal	Definition
1	$\overline{\text{RDY}}$ or $\overline{\text{HLT}}$	Ready or Halt—This line is an unbuffered input to the processor. Pulling this line low causes the processor to suspend operations and to float the buses until it is returned high. The Ready line is available on the 6502 microprocessor while the Halt line is available on the 6800 microprocessor.
2	GND	Ground—This line is the return for system power supplies and signal lines.
3	$\overline{\text{RESET}}$	Reset—The reset line is the unbuffered input to the reset input of the processor. Pulling the reset low causes execution to begin at the location pointed to by the reset vector. A momentary contact push-button switch can be connected to Pins 2 and 3 to perform the reset.
4, 5	UNDF	Undefined—Lines 4 and 5 are unused and allow special functions desired by the user.
6–8	RET, OUT, IN	RS-232C—Lines 6, 7, and 8 provide serial interface to the CPU board using RS-232C signals. Line 7 is the output, line 8 is the input and line 6 is the common return line.
9, 11	TTY PNT (+ and –)	Teletypewriter Printer—These lines provide serial printer interface to the CPU board using a 20-mA loop.
10, 12	TTY KBD (+ and –)	Teletypewriter Keyboard—These lines provide serial keyboard interface to the CPU board using a 20-mA loop.



CHAPTER 13

Benton Harbor Bus to S-100 Bus

A Heath Company H8 system would become more flexible if the wide variety of available S-100-compatible boards could be connected to it. An H8 system owner might also save money by using the competitively priced S-100 boards. This chapter will discuss the conversion of Benton Harbor Bus (BHB) signals to S-100 bus signals.

To accomplish a BHB to S-100 bus conversion, a conversion board is needed. It would fit between the BHB and S-100 buses as shown

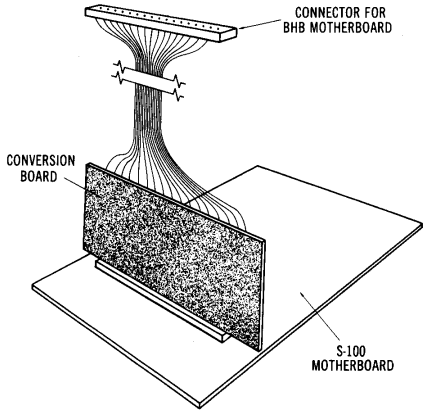


Fig. 13-1. Connection of an S-100 motherboard to a Benton Harbor motherboard via a conversion board.

in Fig. 13-1. The easiest method would be to make the conversion board plug into an S-100 motherboard and to have jumpers run to a connector for the BHB motherboard. The conversion board could be either a printed-circuit or wirewrapped board.

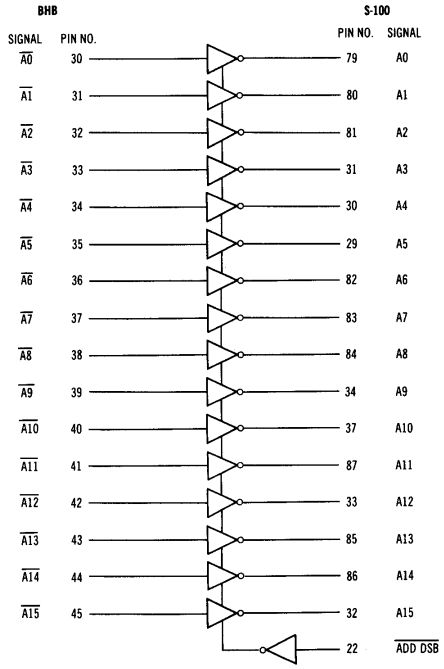


Fig. 13-2. Simple method used to convert the ADDRESS BUS lines.

The Address Bus A0–A15 lines can be converted fairly easily as shown in Fig. 13-2. They only need to be connected to the S-100 lines through 16 inverting three-state buffers. They are also connected to the address disable $\overline{\text{ADD DSB}}$ line through an inverter. If DMA or other bus control devices are not used, the lines could simply be connected through 16 inverters and the $\overline{\text{ADD DSB}}$ line could be omitted.

The BHB data lines $\overline{D0}$–$\overline{D7}$ must be inverted and separated into data-in (DI0–D17) and data-out (DO0–DO7) lines on the S-100 bus. Fig. 13-3 shows a possible conversion of the data bus that is accomplished using 16 inverting three-state buffers. The data output lines can be put in a high-impedance state by $\overline{DO\ DSB}$. However, if DMA is not used, $\overline{DO\ DSB}$ can be omitted and eight inverters used instead. Either type of Read signal (IOR or MEMR) will allow the data input signals to pass inverted to the BHB data lines.

The S-100 status lines are obtained as shown in Fig. 13-4. These lines can be disabled by connecting $\overline{STAT\ DSB}$ to the three-state buffers. Again, without DMA, the $\overline{STAT\ DSB}$ and the buffers can be omitted. On the S-100 bus, status signals are latched onto the bus and remain there until the next machine cycle. In the conversion system shown, the timing will be quite different since these signals are not available on the BHB. The derived lines should have the

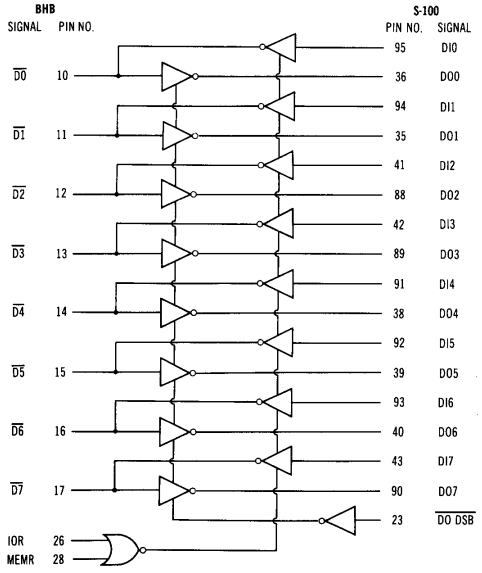


Fig. 13-3. A possible DATA BUS conversion method.

necessary active level at the proper time for most boards used. The two signals, SHLTA and SSTACK, are not obtainable from the BHB but should not restrict the use of memory boards. Also shown in

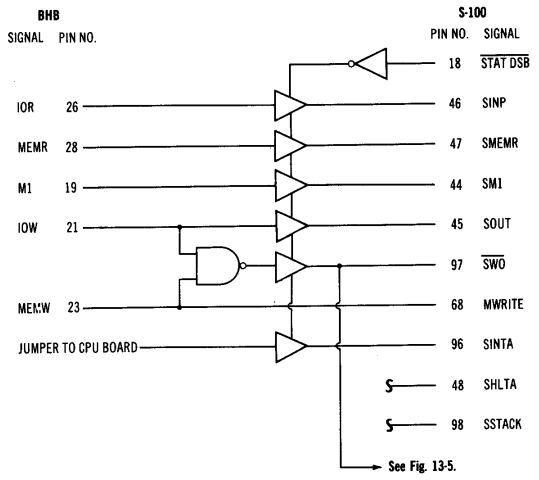


Fig. 13-4. Status line conversion.

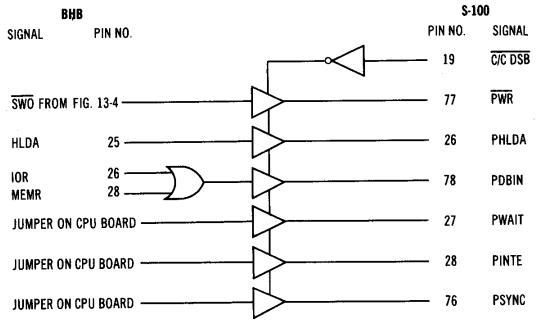


Fig. 13-5. Command/Control line conversion.

Fig. 13-4 is the MWRITE signal. The interrupt acknowledge signal, SINTA, is not obtainable from the BHB but could be jumpered from the H8 CPU board if required.

Fig. 13-5 shows a possible conversion method for obtaining the command/control signals. The lines are shown with three-state buffers which can be omitted if DMA does not require the command/control disable $\overline{C/C\ DSB}$. Signals PSYNC, PWAIT, and PINTE are not obtainable from the BHB; but, if required, they exist on the H8 CPU board and could be jumpered.

A conversion method for the ready and interrupt lines is shown in Fig. 13-6. If either of the S-100 ready lines $\overline{XRDY}$ or $\overline{PRDY}$ goes high, the processor will enter a WAIT state. The BHB has priority interrupts with INT7 being the highest. Interrupts INT1 and INT2 on the BHB are dedicated to the H8 front panel. However, if the front panel is not being used, jumpers can be placed on the H8 CPU board to allow other devices to use INT1 and INT2. One method of handling interrupts is with the H8 priority system shown in Fig. 13-6. This allows five (seven without front panel) priority interrupts. However, if interrupts from peripherals occur on the BHB, the number of lines available will be reduced accordingly. If more interrupts are required, an interrupt-controller board on the S-100 bus could accept VI0–VI7 signals and generate only a $\overline{PINT}$ interrupt signal which would be connected through an inverter to an unused interrupt on the BHB. If an S-100 board has VI0–VI7 active high, then inverters would have to be added to the lines shown in Fig. 13-6.

The remaining bus conversions are shown in Fig. 13-7. The power supplies and ground are straightforward, however, note the higher voltage levels. This is not a problem since the on-board regulators

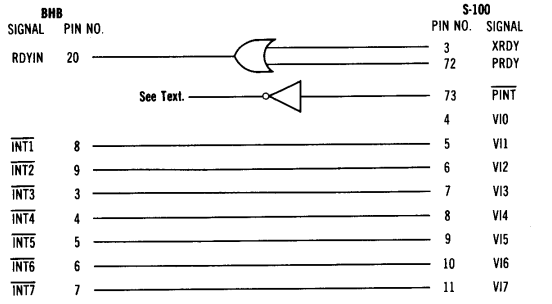


Fig. 13-6. A method that can be used to convert Ready and Interrupt lines.

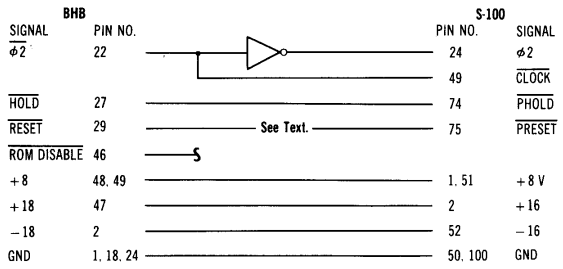


Fig. 13-7. A way to convert miscellaneous buses.

derive the proper voltages from these voltages. The BHB $\phi 2$ clock signal provides both $\overline{\text{CLOCK}}$ and $\phi 2$ through an inverter. The clock can be used as $\phi 1$ on the S-100 bus in most cases but, if true $\phi 1$ is required, an additional nonoverlapping clock circuit will be necessary. The BHB $\overline{\text{HOLD}}$ connects directly to the S-100 $\overline{\text{PHOLD}}$. The BHB $\overline{\text{ROM DISABLE}}$ does not convert to an S-100 signal. Both buses have a reset; $\overline{\text{RESET}}$ on the BHB and $\overline{\text{PRESET}}$ on the S-100. The BHB $\overline{\text{RESET}}$ is a CPU board output which goes low when the CPU RESET is activated, whereas, the S-100 $\overline{\text{PRESET}}$ is a signal to reset the CPU. Connecting these lines together would allow a BHB CPU RESET to also reset any other boards connected to the S-100 bus. Jumpering the S-100 $\overline{\text{PRESET}}$ to $\overline{\text{RESIN}}$ on either the H8 CPU board or the front panel would allow boards on the S-100 bus to reset the CPU.

S-100 Signals not accounted for are PROT (pin 70), RUN (pin 71), UNPROT (pin 20), SSWI (pin 53), PS (pin 69), SS (pin 21), $\overline{\text{EXT CLR}}$ (pin 54), $\overline{\text{PHANTOM}}$ (pin 67), and POC (pin 99). Some of these lines may be implemented with front-panel switches and indicators. Obtaining others may require sophisticated circuitry.

Any effort to use S-100 boards from the BHB, by using a conversion board as discussed, should be preceded by the gathering of as much information as possible about the boards. The required S-100 signals should be determined and compared to either what is available on the conversion board or what can be created elsewhere. Any strict timing of signals must be known to determine if any problems lie therein.

If it is desired to use a conversion board which would permit using BHB boards on an S-100 system, it could be easily accomplished by deriving the lines as on the H8 CPU board. This can be done since the S-100 system was originally designed for the 8080 CPU as is the H8.

CHAPTER 14

TRS-80 Bus to S-100 Bus

The owner of a TRS-80 system might like to use S-100 bus boards because of their lower cost and wider variety. Therefore, this chapter discusses the conversion of signals from the TRS-80 bus to the S-100 bus. A conversion board, either printed circuit or wire-wrapped, is needed. It should be designed to plug into an S-100 motherboard and should be cabled to a connector which fits the TRS-80 expansion edge card.

The Address Bus A0–A15 can be connected direct from the TRS-80 bus to the S-100 bus. If several S-100 boards are used, it might be preferable to buffer the address lines on the conversion board. However, if DMA is used, the buffers should be three-state and be enabled by the $\overline{\text{TEST}}$ (Pin 23) line on the TRS-80 bus (connected through an inverter).

A Data Bus D0–D7 conversion is shown in Fig. 14-1. The data lines are divided into data in (DI0–DI7) and data out (DO0–DO7) for the S-100 bus. Both the data-in and data-out lines are buffered. The $\overline{\text{TEST}}$ line on the TRS-80 bus three-state buffers the data out for DMA operations. The $\overline{\text{RD}}$ and $\overline{\text{IN}}$ lines enable the data in for Read or input operations. If DMA is not needed, the data-out buffers can be omitted *provided* there is not an excessive number of boards on the bus.

The ground lines on the TRS-80 bus (Pins 8, 29, and 37) are connected to the ground lines on the S-100 bus (Pins 50 and 100). However, the TRS-80 bus has only a +5 V power supply, whereas, the S-100 bus has a +8 V and a ±16 V power supply. Therefore, an S-100 motherboard interfaced with a TRS-80 system would have to have separate power supplies.

Fig. 14-2 shows the remainder of the signal conversions. The $\overline{OUT}$, $\overline{WR}$, $\overline{RD}$ and $\overline{IN}$ signals of the TRS-80 are used to derive the SOUT, MWRITE, $\overline{PWR}$, $\overline{SWO}$, SMEMR, SINP, and PDBIN signals of the S-100 bus. These signals will have some timing differences from the true S-100 signals but will work on most boards. The TRS-80 bus has only one interrupt input—$\overline{INT}$. If vectored interrupts are desired, an interrupt controller board can be used on the S-100 bus.

Any device desiring DMA on the S-100 bus activates $\overline{PHOLD}$ and the various disable lines. In the conversion, these lines are ORed to provide the $\overline{TEST}$ signal on the TRS-80 bus. This puts all lines

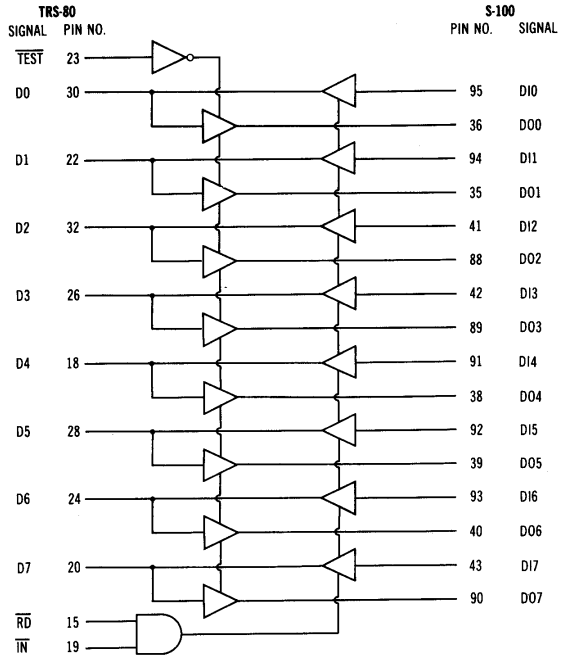


Fig. 14-1. Data line connections for the TRS-80 bus to S-100 bus conversion.

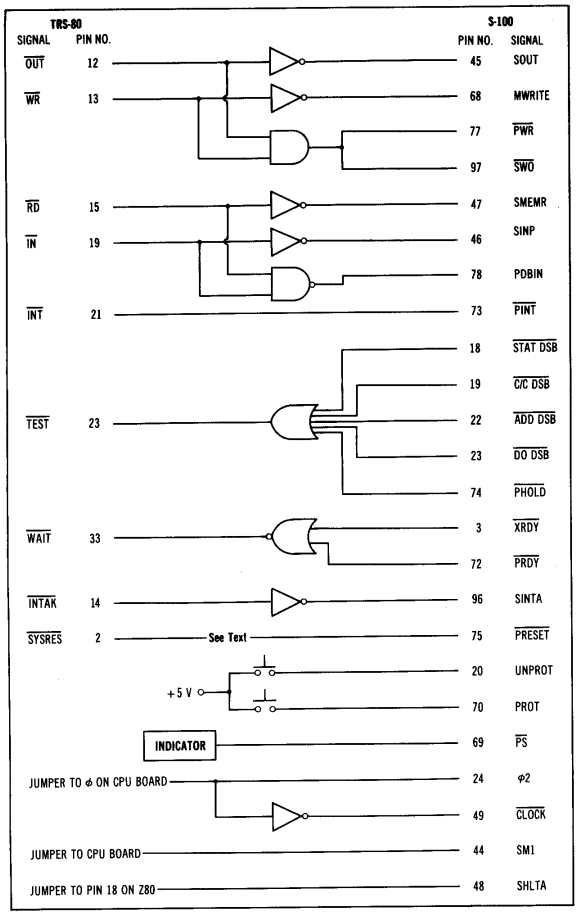


Fig. 14-2. Line connections for the signal conversions not shown in Fig. 14-1.

in a high-impedance state. The Ready lines are combined and connected to the WAIT line on the TRS-80 bus.

On the TRS-80 bus, SYSRES is a signal that resets the peripherals but not the CPU when the reset button is pushed or power is turned on. On the S-100 bus, PRESET is normally used for CPU reset. If the peripherals are to be reset with these lines, they can be connected together, or else SYSRES can be connected to EXT CLR on the S-100 bus. Then EXT CLEAR is used to reset peripherals. The SYSRES line should also be connected to POC since it is active during a power-up condition.

Memory protection can be handled as shown in Fig. 14-2. Front-panel switches will allow setting or resetting the Protect flip-flops while an indicator will permit the monitoring of the status of the flip-flops.

There are no timing signals on the TRS-80 bus but, by using jumpers to the TRS-80 CPU board, the $\phi 2$, CLOCK and SM1 signals can be derived for the S-100 bus if needed. Also, $\phi 1$ can be derived from $\phi 2$ by using a nonoverlapping clock circuit. The Halt Acknowledge instruction SHLTA could also be jumpered. S-100 signals PWAIT, PINTE, PSYNC, and SSTACK are not derivable from the Z80-based TRS-80. However, the PHLDA signal could be jumpered from the Z80 BUSAK.

Building a conversion board for use in connecting the TRS-80 to the S-100 should be preceded by obtaining complete information on the S-100 boards. This information is used to determine which of the lines are required and which can be omitted. A few boards require some signals not derivable from the TRS-80 and, therefore, may not be usable. The timing of the derived signals is different from normal S-100 timing and, thus, boards with strict requirements may not work.

A conversion board to allow use of TRS-80 boards on S-100 systems is possible as most of the signals on the TRS-80 bus are readily derived. However, the CAS and MUX signals which are used for 16-pin dynamic memory are not available and, therefore, an additional timing circuit to generate these signals must be included. See Chapter 5 and Fig. 5-6 for a description of a TRS-80 circuit that will generate these signals.

CHAPTER 15

6502/6800 to S-100 Conversion

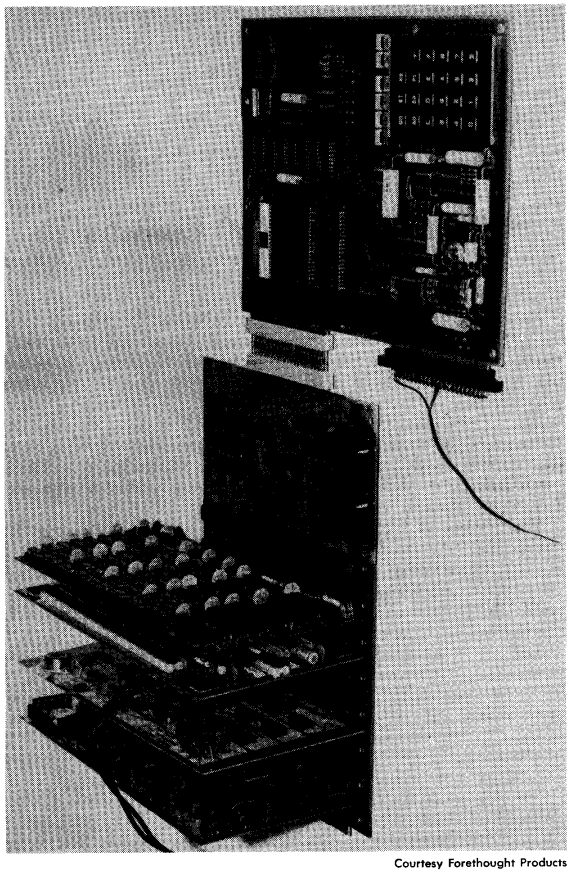
Although 6502/6800-based systems have been quite popular, relatively few expansion boards have been produced for them. Only the SS-50 bus offers users a variety of boards. However, use of the plentiful S-100 boards on 6502/6800 systems is possible via a bus interface board.

The KIMSI, shown in Figs. 15-1 and 15-2, is a good, commercially produced KIM to S-100 interface board that will be used to illustrate the needed signal conversions. The KIMSI interface board plugs onto the KIM expansion connector and provides an eight-slot S-100 motherboard.

Three types of signals (Address, Data, and Control) must be transferred between the buses. Since it is not provided on-board, all KIM signals must be buffered. Both systems use 16-line address buses so the A0–A15 signals of the 6502 translate directly into the S-100 address lines as shown in Fig. 15-3. The 74367 buffers provide the needed drive.

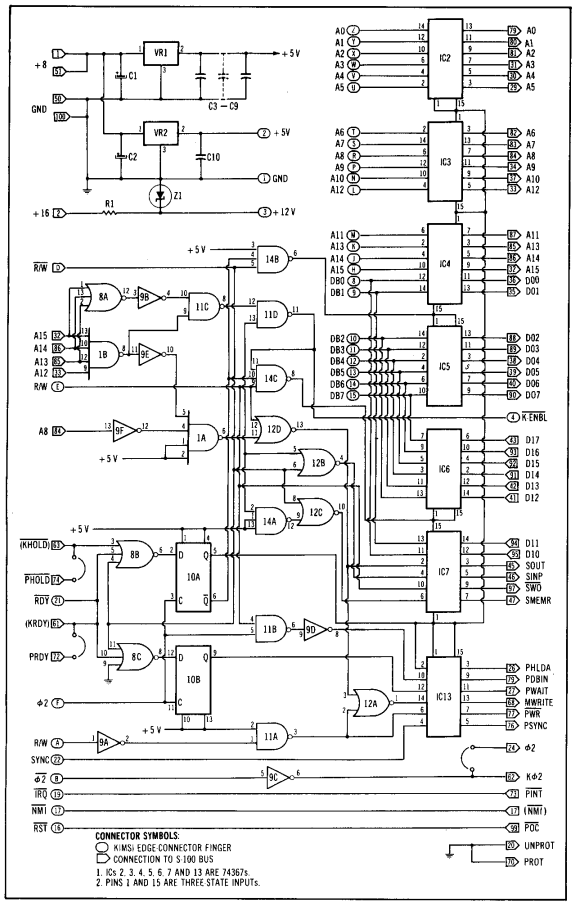
The bidirectional data bus of the 6502 must be divided into data-in and data-out lines as shown in Fig. 15-4. Data out and data in are both connected to the D0–D7 lines of the 6502 through three-state buffers. The data-out buffers are controlled by the $\overline{R/W}$ line of the KIM and the data-in buffers are controlled by the R/W line of the KIM. The possibility of input and output data appearing on the D0–D7 lines simultaneously is, therefore, prevented.

The $\phi 2$ line of the 6502 is inverted to become the S-100 $\phi 2$ line and can be jumpered to K$\phi 2$. The SYNC signal of the 6502 which occurs at the beginning of each op code fetch cycle is buffered and becomes PSYNC for the S-100. However, the PSYNC signal occurs at the beginning of each 8080 machine cycle so the conversion does



Courtesy Forethought Products

Fig. 15-1. The KIMSI interface board.



Courtesy Forethought Products

Fig. 15-2. Schematic of the KIMSI board.

not work since more than one PSYNC signal occurs during the execution of an instruction. The SYNC signal could be better translated into SM1 (line 44) which occurs at the beginning of each 8080 op code fetch.

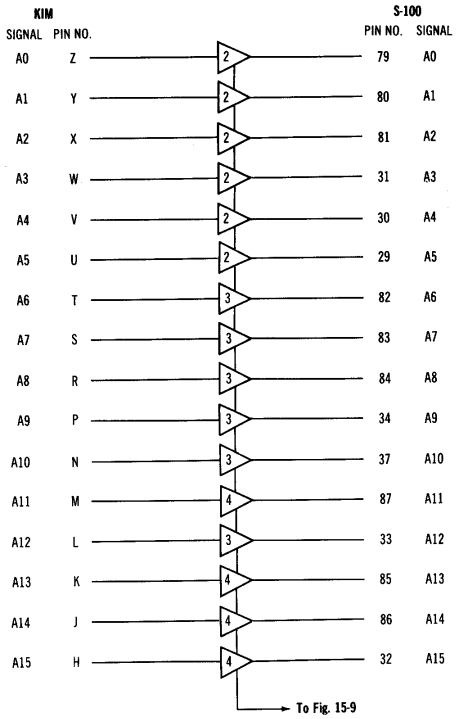


Fig. 15-3. The address lines are simply buffered lines.

Fig. 15-5 shows the derivation of the PDBIN signal which occurs during the $\phi 2$ cycle when the 6502 is in a Read operation. The R/W line of the 6502 is buffered and becomes the $\overline{\text{PWR}}$ line for the S-100. Also, the R/W line of the KIM is buffered and becomes

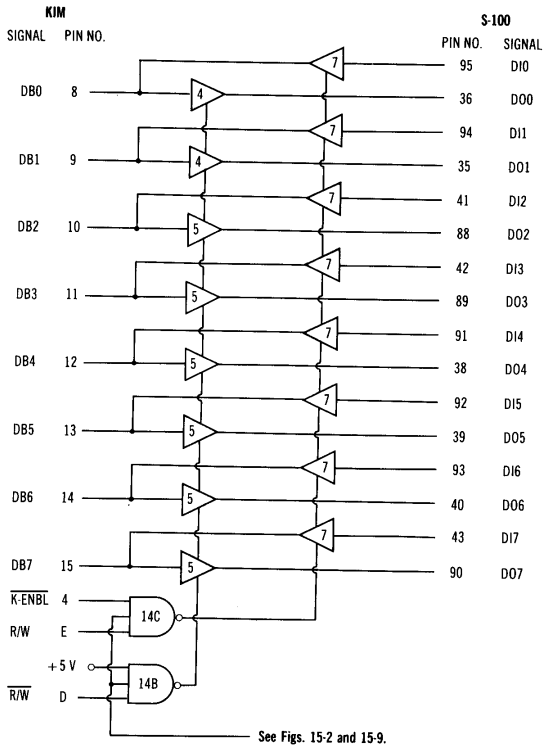


Fig. 15-4. The data lines of the KIM must be split.

the $\overline{\text{SWO}}$ line for the S-100. Timing of these signals is generally acceptable to most S-100 boards.

The input and output status lines are derived in Fig. 15-6. The 6502-based system treats memory and I/O devices alike. Both are assigned addresses between Hex 0000 and FFFF and both must respond to its Read/Write line. The S-100 employs separate memory and I/O Read/Write lines, thus allowing up to 512 special I/O port

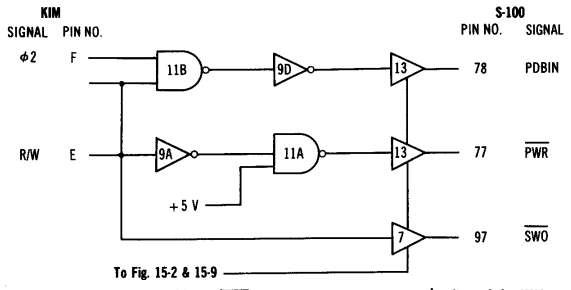


Fig. 15-5. The PDBIN, $\overline{\text{PWR}}$ and $\overline{\text{SWO}}$ lines are derived from the R/W line of the KIM.

addresses. The KIMSI interface board provides these special addresses by reserving one section of memory for I/O ports. These locations cannot be assigned to memory and are the only S-100 I/O locations available. When lines A12–A15 are high and line A8 is low, the decoder circuitry produces a low out of NAND gate 1A. This low is combined with the R/W of the 6502 to generate the SOUT and with the $\overline{\text{R/W}}$ of the 6502 to obtain SINP. Both SOUT and SINP will be active any time an address consisting of FYXX (where Y is even) is called. The I/O devices will respond to F0XX, F2XX, F4XX, F6XX, F8XX, FAXX, FCXX, and FEXX. Normally all I/O boards are assigned an F0XX address. F2XX, F4XX, . . . are reserved for those I/O boards that respond to the upper address lines (A8–A15). To prevent enabling two boards at the same time, a board at F000 and a board at F200, one F0XX address must be disallowed for boards using F0XX locations. Boards responding to the high byte, F2XX, etc., must use that disallowed low byte in their address. If

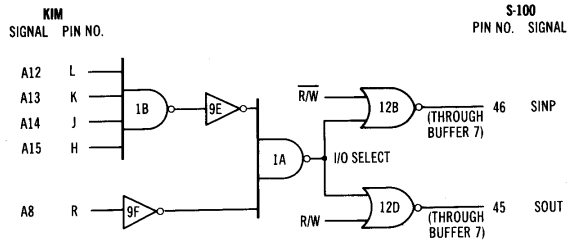


Fig. 15-6. Derivation of the input and output status lines.

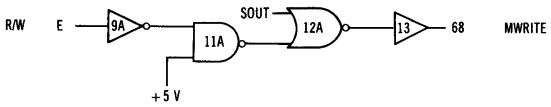


Fig. 15-7. The MWRITE is derived from the I/O select.

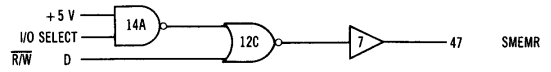


Fig. 15-8. The SMEMR is derived from the I/O select.

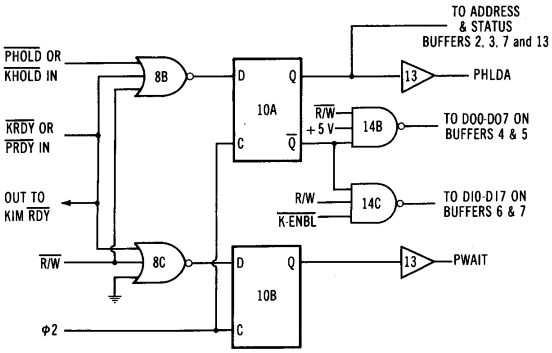


Fig. 15-9. The Hold and Ready interface circuitry.

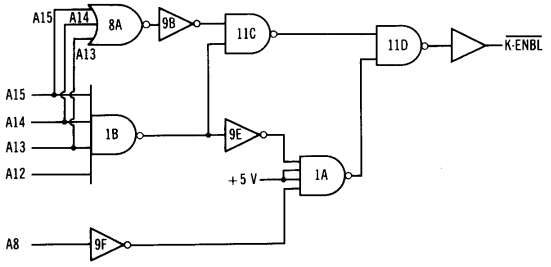
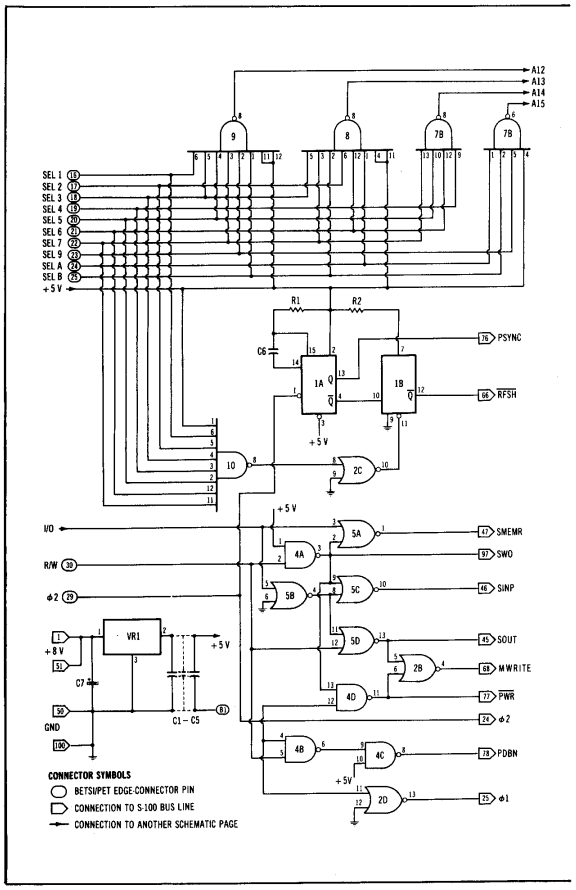
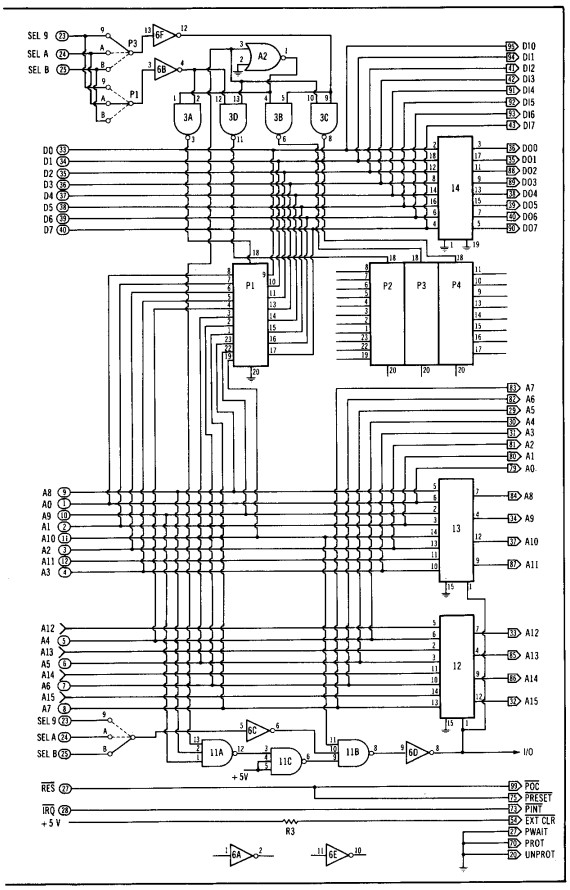


Fig. 15-10. Decoder circuitry used by the KIMSI interface board to enable the KIM-1.



(A) Part 1.

Fig. 15-11. The schematic for



(B) Part 2.

Courtesy Forethought Products

the BETSI interface board.

F000, for example, is the forbidden address, conflicts will not occur as high byte boards will be at F200, F400, etc.

The MWRITE is also a product of the circuitry of Fig. 15-7. The SOUT line is NORed with the R/W of the 6502 which produces an output to memory when the I/O section has not been enabled. By combining the I/O select signal from gate 1A with the $\overline{R/W}$ of the 6502, SMEMR is obtained as shown in Fig. 15-8. By deriving the MWRITE and SMEMR from the R/W and I/O select circuitry, memory and I/O addresses are separated.

The Hold and Ready interface circuitry is shown in Fig. 15-9. The S-100 $\overline{KRDY}$ and $\overline{PRDY}$ lines are directly connected to the $\overline{RDY}$ input of the 6502. The PWAIT signal is produced by IC 10B during the $\phi 2$ cycle of 6502, following the $\phi 1$ cycle in which the $\overline{KRDY}$ or the $\overline{PRDY}$ is pulled low. The $\overline{KRDY}$ or $\overline{PRDY}$ will stop the 6502 from allowing the use of slow memory. The $\overline{KHOLD}$ and $\overline{PHOLD}$ can be used by DMA devices to gain control of the buses. The $\overline{RDY}$ line of the 6502 must be used in conjunction with the Hold lines. Pulling the Hold and Ready lines low floats the Address, Data, and Control lines during the next Read cycle.

The $\overline{PINT}$ line connects directly to the $\overline{IRQ}$ input of the 6502. The $\overline{NMI}$ line of 6502 is fed directly by S-100 line 17 which is not standardized in most 8080-based systems. The $\overline{POC}$ line of the S-100 is connected to and resets the 6502 through the $\overline{RST}$ line. The Protect and Unprotect lines are unused on the KIMSI interface board but could be implemented with front-panel switches and indicators. The KIMSI board uses the unregulated S-100 voltages to obtain the regulated +5 V and +12 V required by the KIM-1 microcomputer.

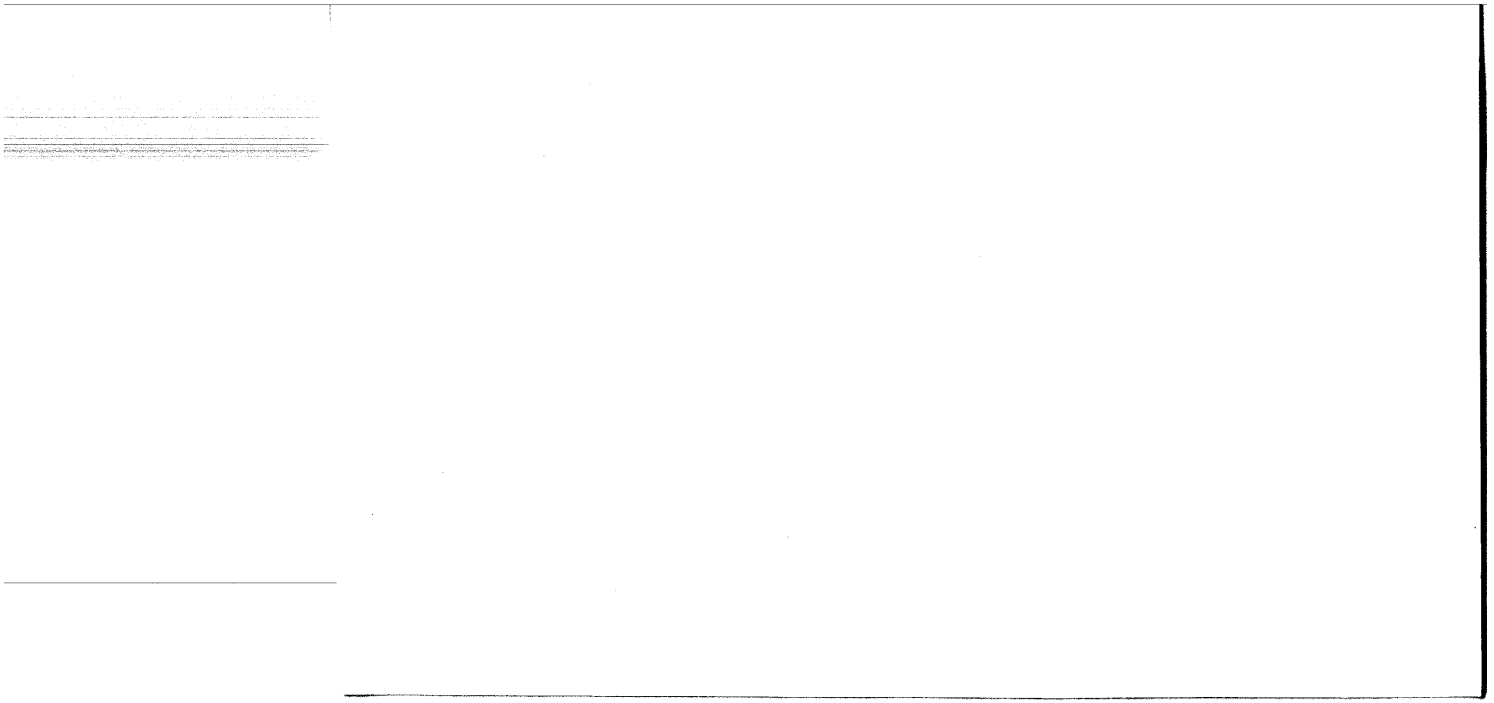
Because the KIM-1 microcomputer has its monitor ROMs and 1 kilobyte of RAM on board, the KIMSI interface board must look at the address lines and select the on-board memory when it is called by the processor. The $\overline{K\text{-}ENBL}$ line, when pulled low, enables on-board memory and, when high, disables on-board memory. The KIM-1 microcomputer reserves Hex locations 0000 to 1FFF and FFF0 to FFFF for its use. The decoder circuitry used by the KIMSI interface board to enable the on-board memory of the KIM is shown in Fig. 15-10. Without the $\overline{K\text{-}ENBL}$, more than one device could be on the data bus at the same time.

The circuitry used on the KIMSI board can easily be adapted for use by other 6502-based systems. Forethought Products produces a PET to S-100 interface board, the BETSI, which is shown schematically in Fig. 15-11. Notice that although some lines are handled differently, most of the same S-100 signals are derived.

Since the 6502 and 6800 processors produce the same Clock, Address, Data, R/W, Interrupt, and Reset lines, they are con-

verted as previously discussed. The Ready line is not available on the 6800 and slow memory must stretch its clock cycles. The 6800 microprocessor outputs a valid memory-address signal, VMA, each time a memory or I/O operation begins which can be used as the S-100 SYNC. The 6800 $\overline{\text{HALT}}$ input can be connected to the S-100 $\overline{\text{HOLD}}$ lines to allow DMA operations. The three-state control (TSC) of the 6800 is functionally the same as the S-100 address disable $\overline{\text{ADDR DSBL}}$. They must, however, be connected through an inverter. The S-100 data-out disable ($\overline{\text{DO SB}}$) function can be performed with the data-bus enable line (DBE) of the 6800 microprocessor, if the $\overline{\text{DB DSB}}$ is inverted. The bus available (BA) output of the 6800 can be used as the S-100 hold acknowledge (PHLDA) signal, in response to a PHOLD or KHOLD input.

The conversion from the 6502/6800 buses to the S-100 bus is not difficult for most signals. Timing and signal information should be carefully examined, however, before any board is added.



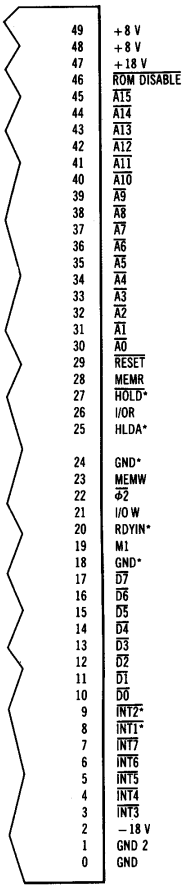
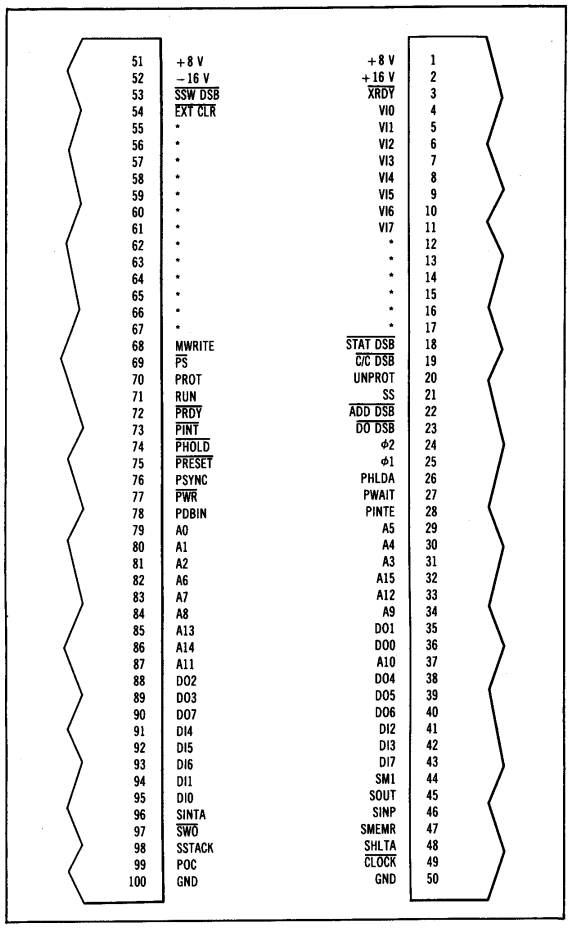


Fig. A-2. The Benton Harbor Bus pin designations.



51	+8 V	+8 V	1
52	−16 V	+16 V	2
53	SSW DSB	XRDY	3
54	EXT CLR	VI0	4
55	*	VI1	5
56	*	VI2	6
57	*	VI3	7
58	*	VI4	8
59	*	VI5	9
60	*	VI6	10
61	*	VI7	11
62	*	*	12
63	*	*	13
64	*	*	14
65	*	*	15
66	*	*	16
67	*	*	17
68	MWRITE	STAT DSB	18
69	PS	C/C DSB	19
70	PROT	UNPROT	20
71	RUN	SS	21
72	PRDY	ADD DSB	22
73	PINT	DO DSB	23
74	PHOLD	Φ2	24
75	PRESET	Φ1	25
76	PSYNC	PHLDA	26
77	PWR	PWAIT	27
78	PDBIN	PINTE	28
79	A0	A5	29
80	A1	A4	30
81	A2	A3	31
82	A6	A15	32
83	A7	A12	33
84	A8	A9	34
85	A13	DO1	35
86	A14	DO0	36
87	A11	A10	37
88	DO2	DO4	38
89	DO3	DO5	39
90	DO7	DO6	40
91	DI4	DI2	41
92	DI5	DI3	42
93	DI6	DI7	43
94	DI1	SM1	44
95	DI0	SOUT	45
96	SINTA	SINP	46
97	SWO	SMEMR	47
98	SSTACK	SHLTA	48
99	POC	CLOCK	49
100	GND	GND	50

Fig. A-1. The S-100 pin designations.

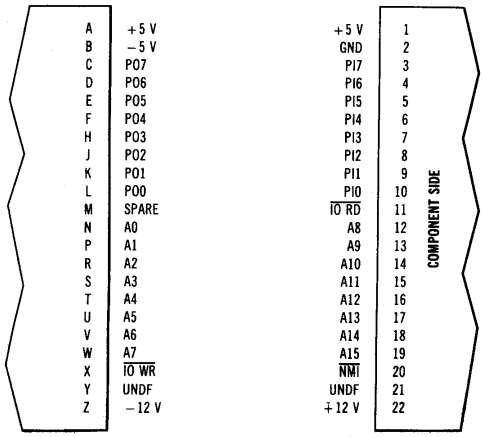


Fig. A-6. Pin designations for the Digital Group I/O board.

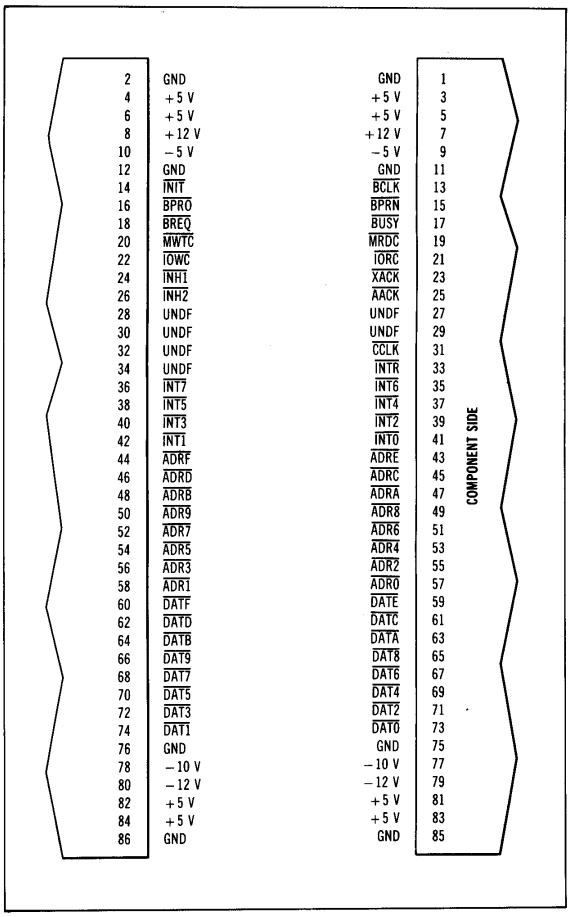


Fig. A-3. The SBC pin designations.

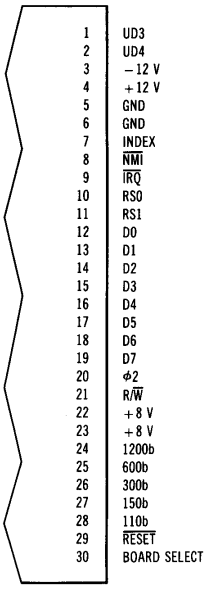


Fig. A-8. The SS-30 pin designations.

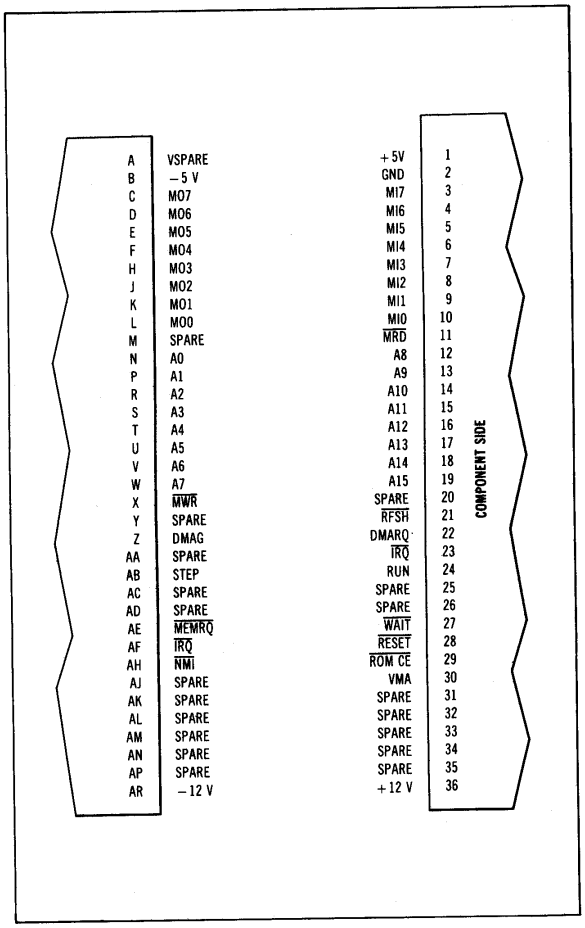


Fig. A-5. Pin designations for the Digital Group memory board.

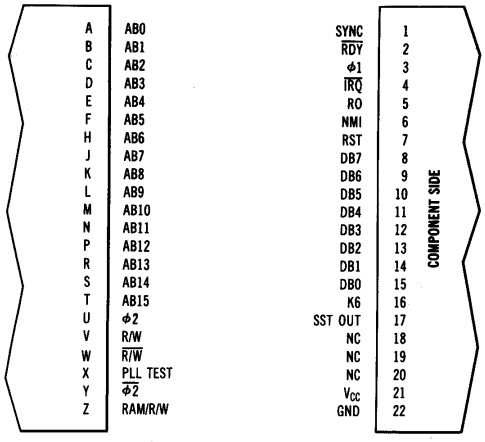


Fig. A-10. The KIM-1 expansion-board pin designations.

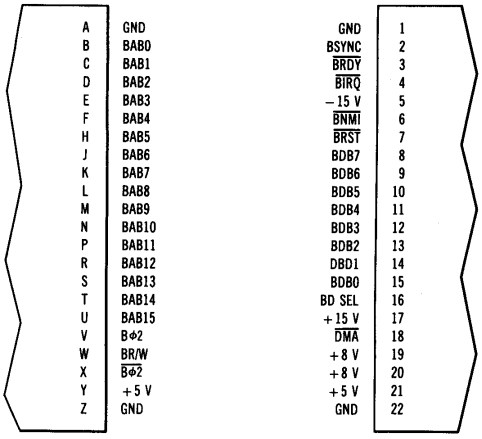


Fig. A-11. The KIM-4 pin designations.

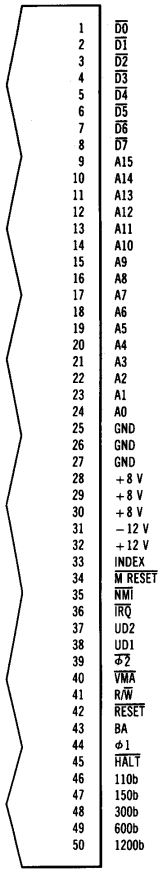


Fig. A-7. The SS-50 pin designations.

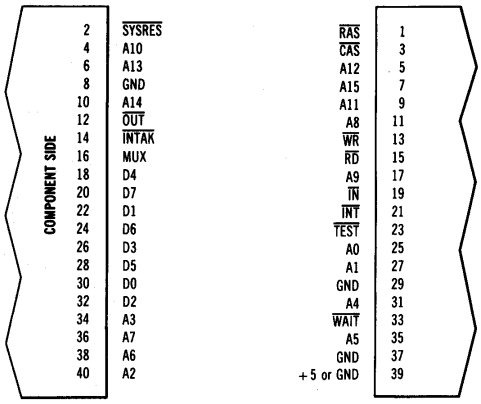
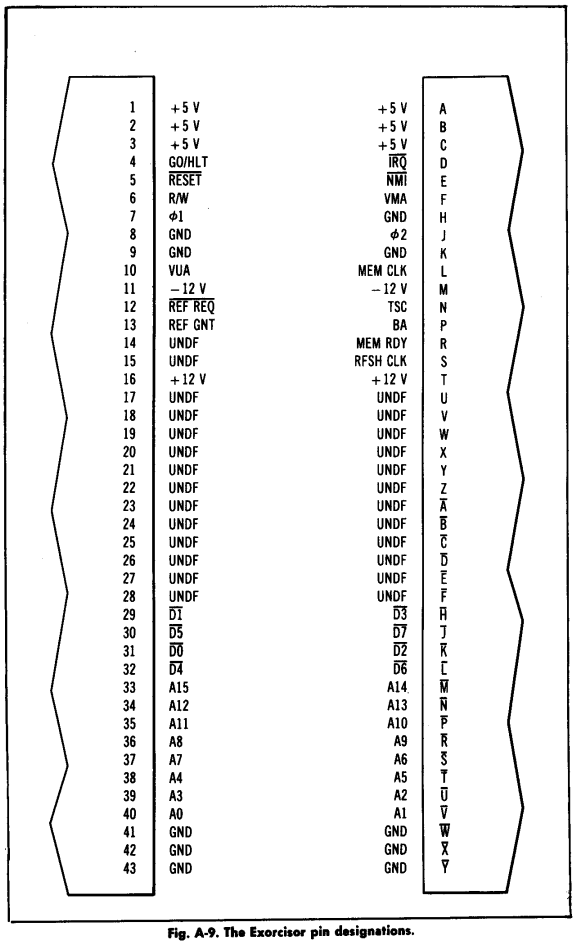


Fig. A-4. The TRS-80 pin designations.



1	+5 V	+5 V	A
2	+5 V	+5 V	B
3	+5 V	+5 V	C
4	GO/HLT	$\overline{IRQ}$	D
5	$\overline{RESET}$	$\overline{NMI}$	E
6	R/W	VMA	F
7	ϕ1	GND	H
8	GND	ϕ2	J
9	GND	GND	K
10	VUA	MEM CLK	L
11	−12 V	−12 V	M
12	$\overline{REF\ REQ}$	TSC	N
13	REF GNT	BA	P
14	UNDF	MEM RDY	R
15	UNDF	RFSH CLK	S
16	+12 V	+12 V	T
17	UNDF	UNDF	U
18	UNDF	UNDF	V
19	UNDF	UNDF	W
20	UNDF	UNDF	X
21	UNDF	UNDF	Y
22	UNDF	UNDF	Z
23	UNDF	UNDF	$\overline{A}$
24	UNDF	UNDF	$\overline{B}$
25	UNDF	UNDF	$\overline{C}$
26	UNDF	UNDF	$\overline{D}$
27	UNDF	UNDF	$\overline{E}$
28	UNDF	UNDF	$\overline{F}$
29	$\overline{D1}$	$\overline{D3}$	$\overline{H}$
30	$\overline{D5}$	$\overline{D7}$	$\overline{J}$
31	$\overline{D0}$	$\overline{D2}$	$\overline{K}$
32	$\overline{D4}$	$\overline{D6}$	$\overline{L}$
33	A15	A14	$\overline{M}$
34	A12	A13	$\overline{N}$
35	A11	A10	$\overline{P}$
36	A8	A9	$\overline{R}$
37	A7	A6	$\overline{S}$
38	A4	A5	$\overline{T}$
39	A3	A2	$\overline{U}$
40	A0	A1	$\overline{V}$
41	GND	GND	$\overline{W}$
42	GND	GND	$\overline{X}$
43	GND	GND	$\overline{Y}$

Fig. A-9. The Exorcisor pin designations.

APPENDIX

Pinout Designations

The various pinout designations given throughout the book are listed again in this appendix. They will serve here as a convenient finger-tip guide to the pin designations.

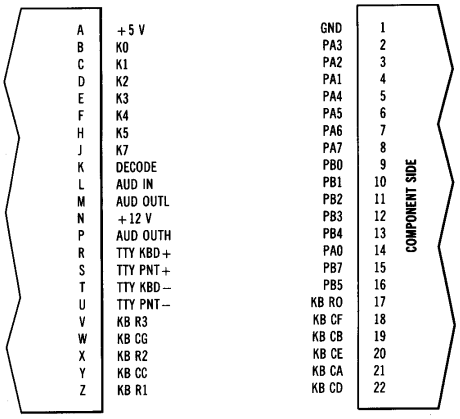


Fig. A-12. The KIM-1 application-connector pin designations.

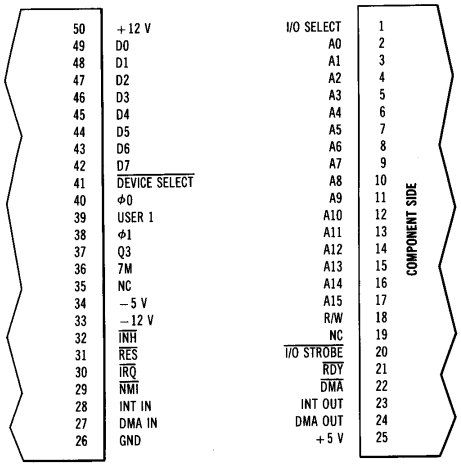


Fig. A-13. The Apple II pin designations.

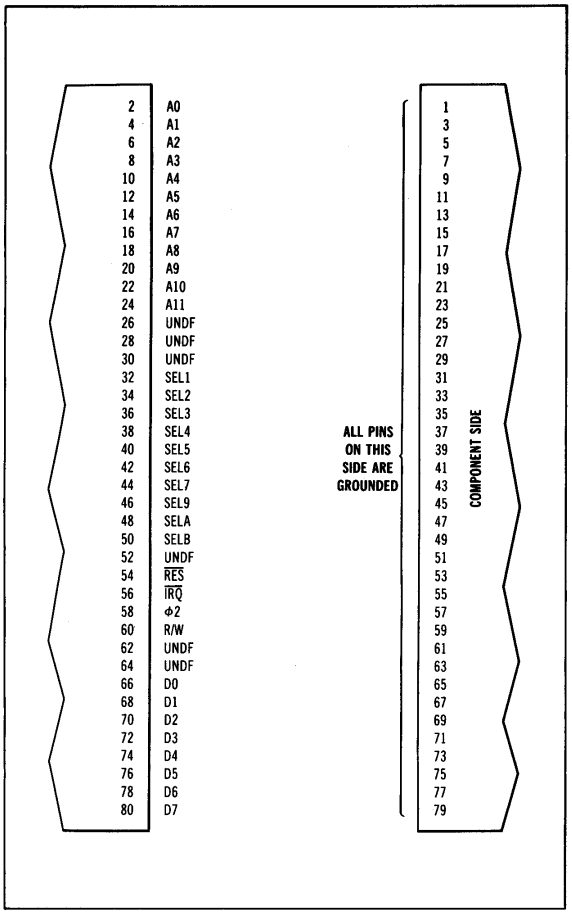


Fig. A-14. The PET expansion-connector pin designations.

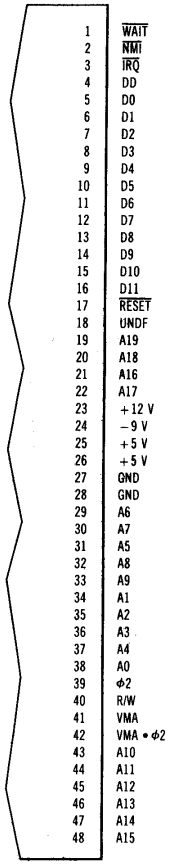


Fig. A-15. The Ohio Scientific Bus pin designations.